

COMPAL CONFIDENTIAL

MODEL NAME : ZAM81  
PCB NO : LA-A913P  
BOM P/N :  
GPIO MAP: 3.1


Huston 15" DSC  
Broadwell U

2013-08-20  
REV : 0.1 (X00)

@ : Nopop Component  
EMC@ : EMI, ESD and RF Component  
@EMC@ : EMI, ESD and RF Nopop Component  
XDP@ : XDP Component  
CONN@ : Connector Component

MB PCB	
Part Number	Description
DAA0007Y000	PCB 13N LA-A913P RRV0 MB DSC DOCK 3

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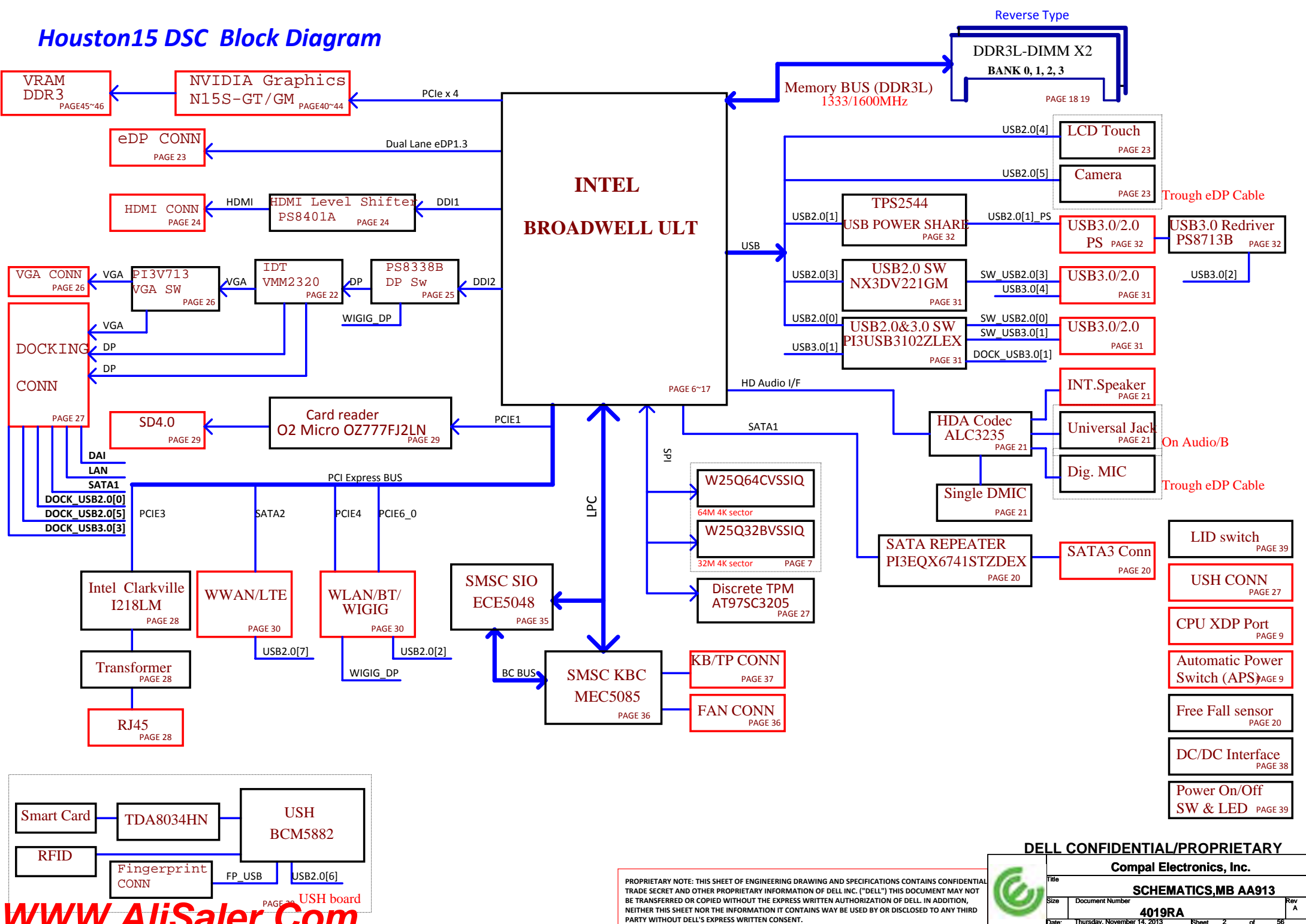
**SCHEMATICS,MB AA913**

**4019RA**

Rev **A**

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# Houston15 DSC Block Diagram



WWW.AliSaler.Com

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and  
PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			GPU/WIGIG
PCIE 6		SATA 3	WIGI/Express
		SATA 2	mSATA/PCIE
		SATA 1	HDD
		SATA 0	DOCK

BDW ULT	USB PORT#	DESTINATION
	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA

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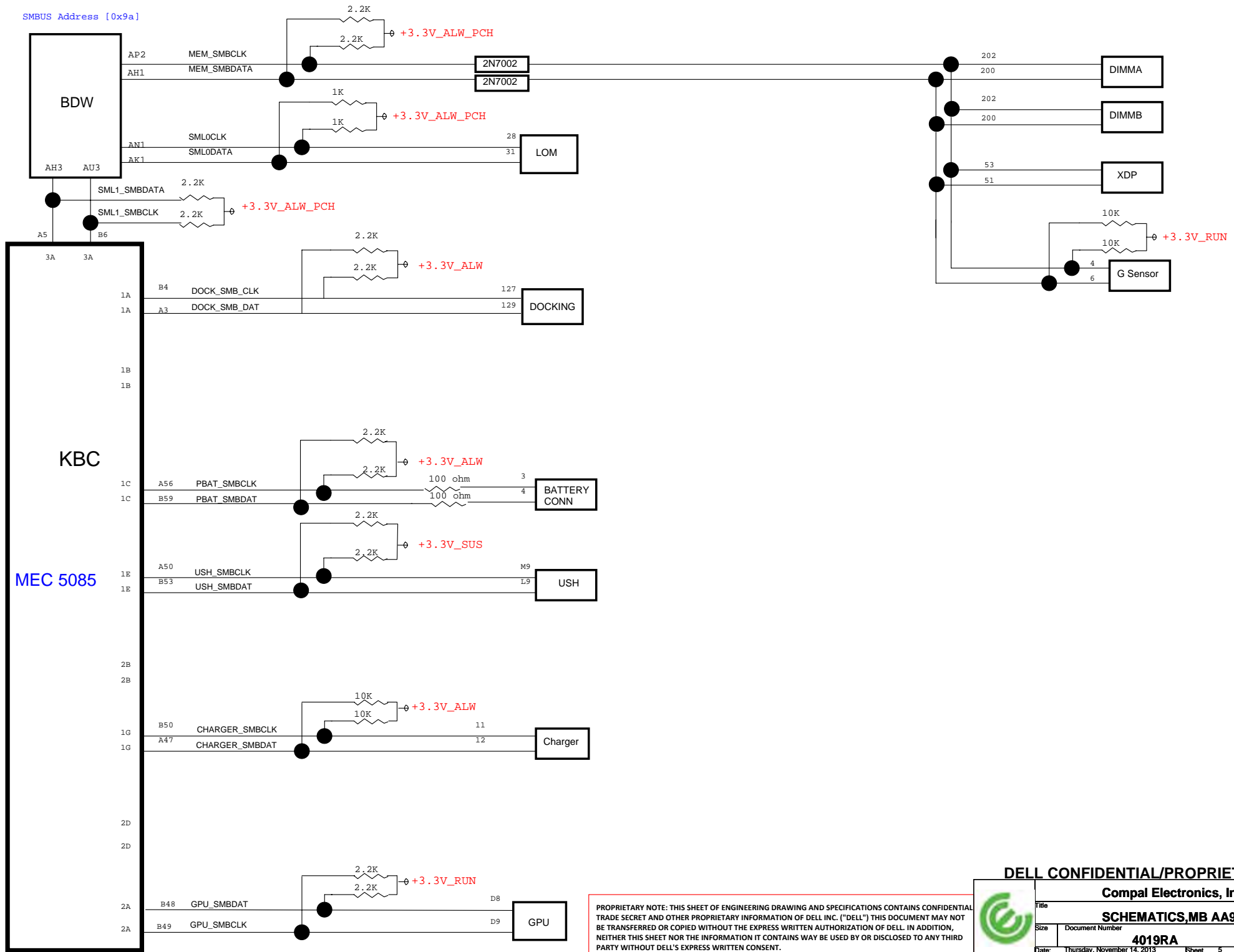


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SMBUS Address [0x9a]



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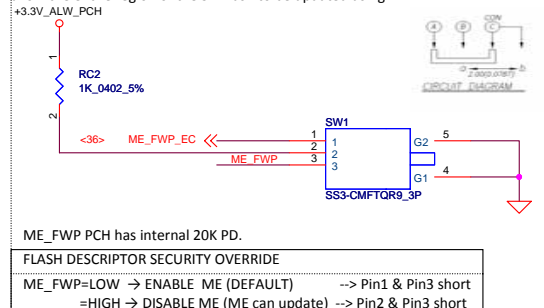
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## DSC SATA port

Service Mode Switch:  
Add a switch to ME\_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



ME\_FWP\_PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

ME\_FWP=LOW -> ENABLE ME (DEFAULT) -> Pin1 & Pin3 short  
=HIGH -> DISABLE ME (ME can update) -> Pin2 & Pin3 short

SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H12 Entry	NA	NA
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H14D_En	NA	M2 3030 WIGIG
NA	HDD	H14U_En	NA	NA
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)
NA	HDD	H15D_En	NA	M2 3030 WIGIG
NA	HDD	H15U_En	NA	Express card

contact to WWAN

SATA2/PCIE6\_L1 contact to WWAN  
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

contact to WLAN

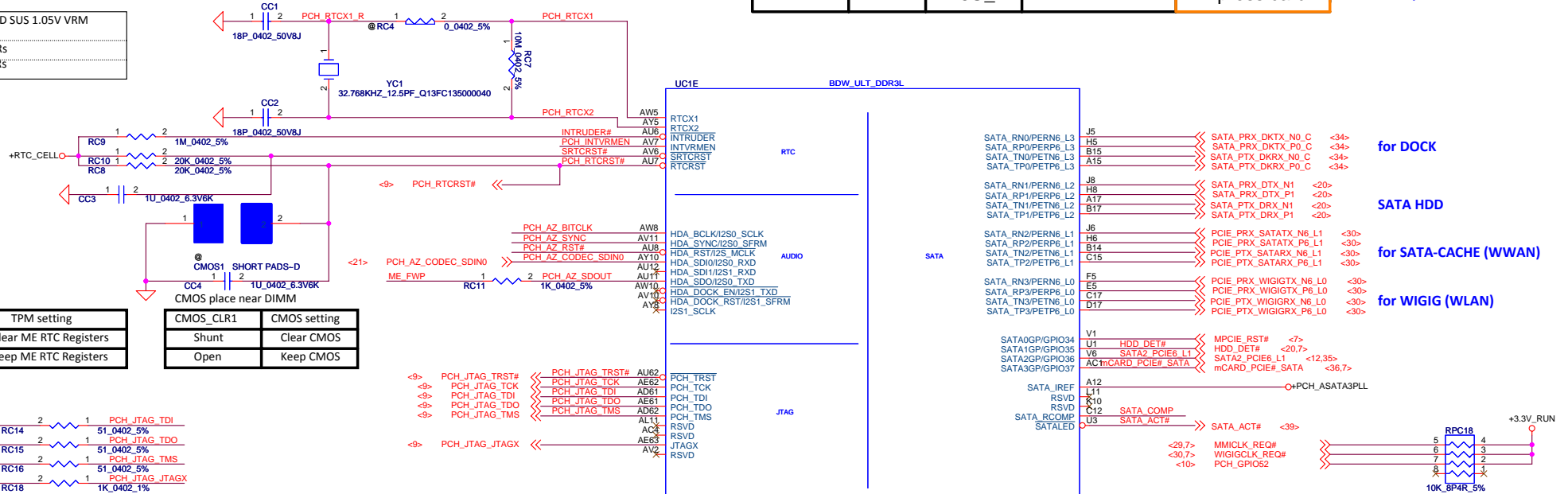
SATA2/PCIE6\_L1 contact to WWAN  
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

contact to WLAN

contact to Express card

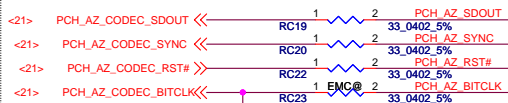
INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs



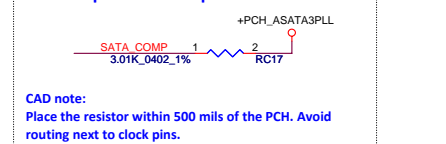
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

## HDA for Codec



## SATA Impedance Compensation



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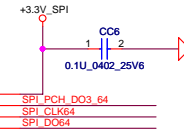


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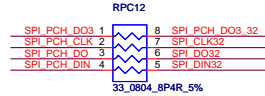
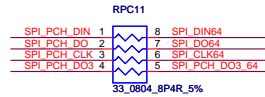
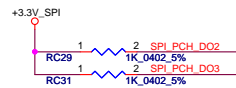
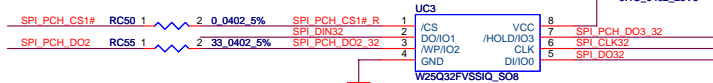
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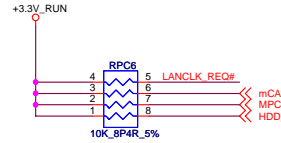
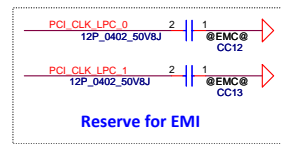
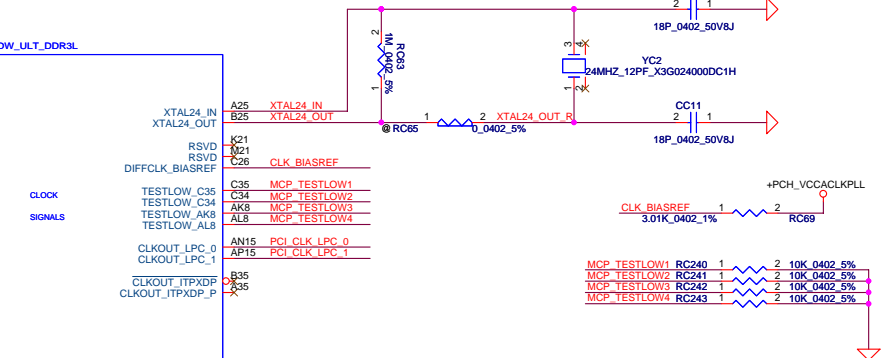
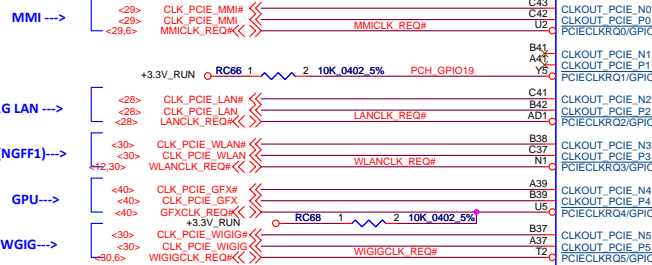
### 64Mb Flash ROM



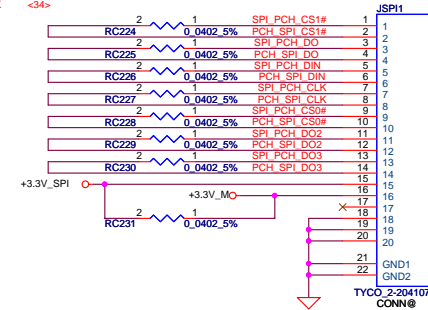
The diagram shows the connection of two SPI\_PCH signals to a U3C component. On the left, two signals are defined: SPI\_PCH\_CS# with a value of RC50 1 and SPI\_PCH\_DO2 with a value of RC55 1. Each signal is connected to a resistor (indicated by a zigzag line) with a value of 2. The SPI\_PCH\_CS# resistor is connected to pin 2 of the U3C component, which is labeled SPI\_PCH\_CS# R. The SPI\_PCH\_DO2 resistor is connected to pin 33 of the U3C component, which is labeled SPI\_PCH\_DO2 32. The U3C component is a rectangular block with pins 1 through 8. Pin 1 is labeled VCC, pin 2 is labeled /CS, pin 3 is labeled DO/IO1, pin 4 is labeled /WP/IO2, pin 5 is labeled DI/IO, pin 6 is labeled CLK, pin 7 is labeled VCC, and pin 8 is labeled SPI\_PCH\_DO3 32. The U3C component is also connected to a W25Q32FVSS1Q\_008 component, which is a rectangular block with pins 1 through 8. Pin 1 is labeled VCC, pin 2 is labeled /CS, pin 3 is labeled DO/IO1, pin 4 is labeled /WP/IO2, pin 5 is labeled DI/IO, pin 6 is labeled CLK, pin 7 is labeled VCC, and pin 8 is labeled SPI\_PCH\_DO3 32.



UC1F	BDW_ULT_DDR3
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PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card



support SPI TPM	
LPC_0	LPC_1
SIO	DOCK
MEC	DEBUG

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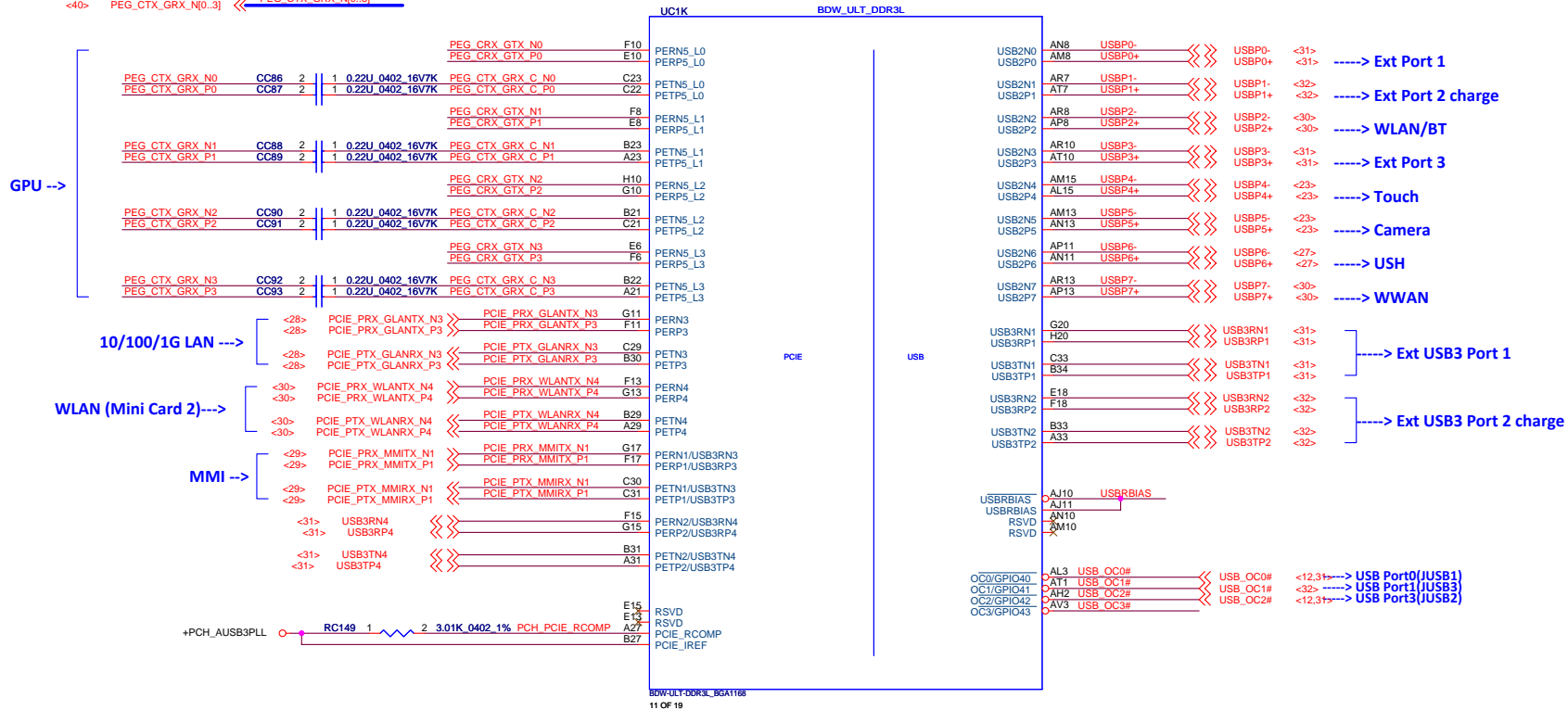






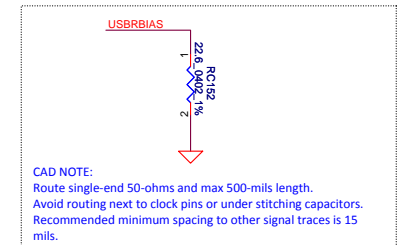
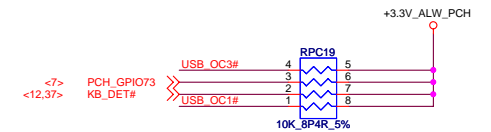
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<40> PEG\_CTX\_GRX\_P[0..3] << PEG\_CTX\_GRX\_P[0..3]  
<40> PEG\_CTX\_GRX\_N[0..3] << PEG\_CTX\_GRX\_N[0..3]

## PCIe for DSC



PCB	USB2 7
H12 UMA	WWAN
H12 Entry	NA
H14 DSC	WWAN
H14 UMA	WWAN
H14D_En	NA
H14U_En	NA
H15 DSC	WWAN
H15 UMA	WWAN
H15D_En	NA
H15U_En	Express

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	Express card

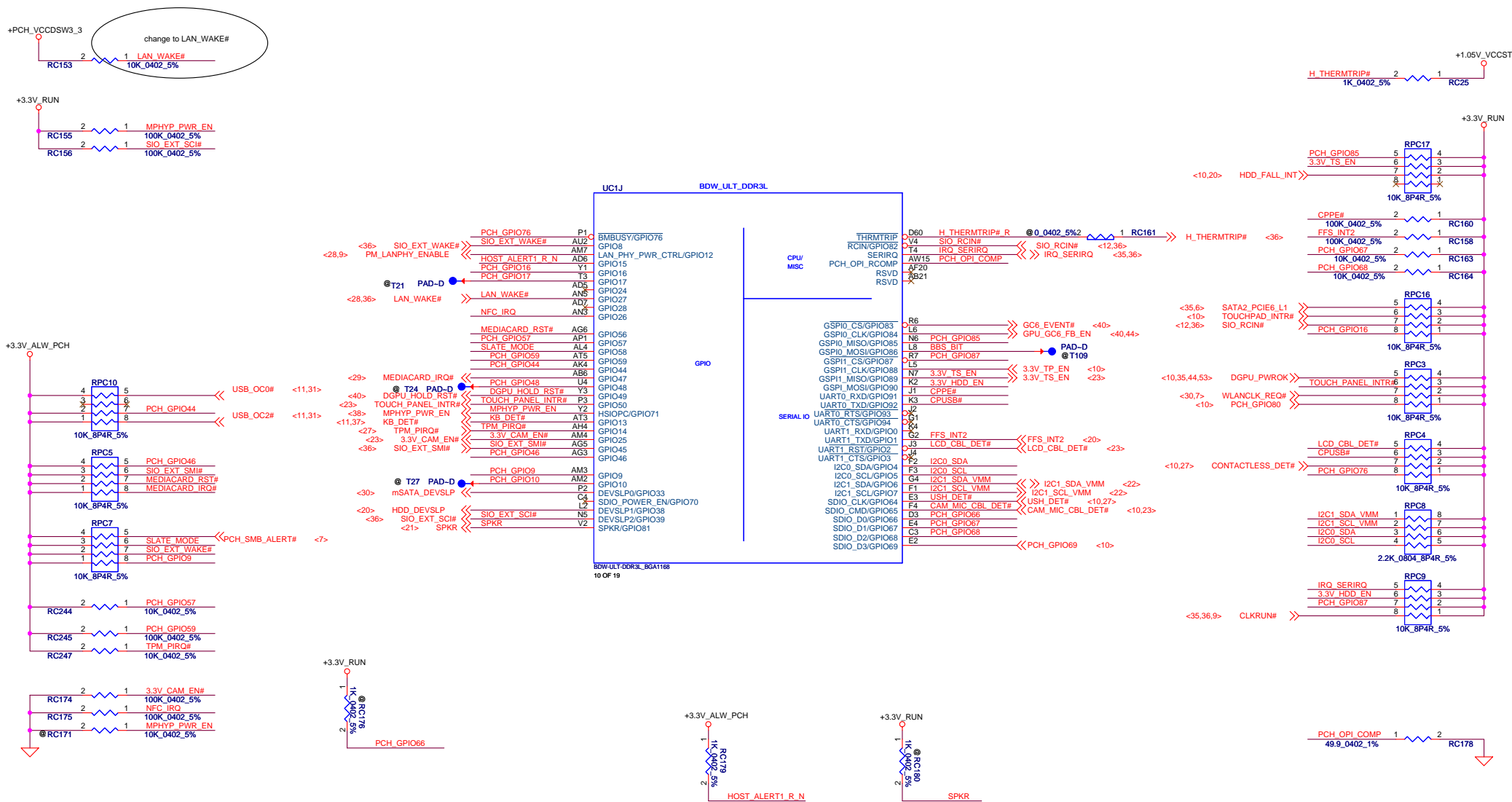


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TOP-BLOCK SWAP OVERRIDE	
HIGH depop RC288	
LOW pop RC288 (DEFAULT)	

BOOT BIOS STRAP BIT BBS	
HIGH	LPC
LOW(DEFAULT)	SPI

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

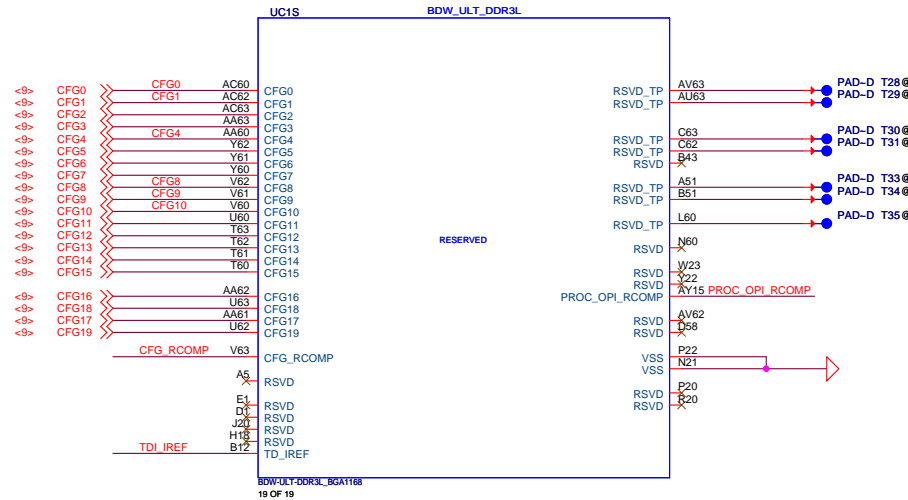
NO REBOOT STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

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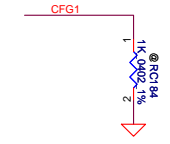
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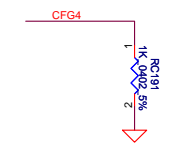
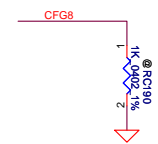
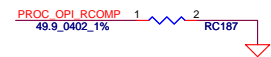
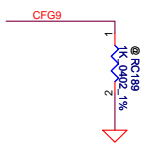
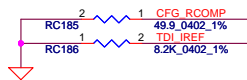
## CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed



PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0:Disable Noa will be available pegrardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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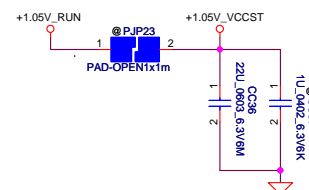
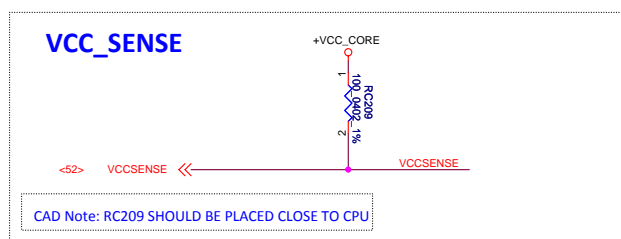
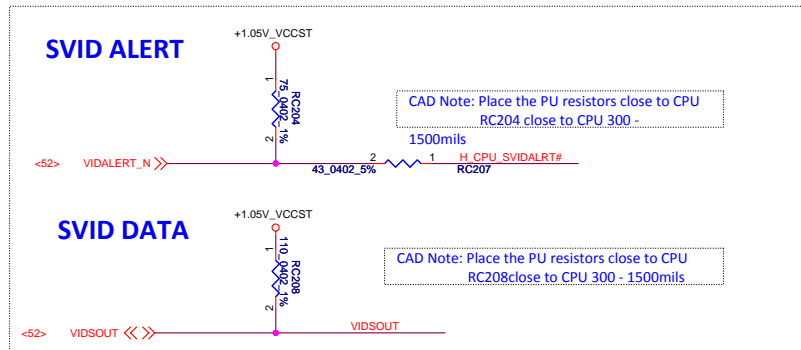
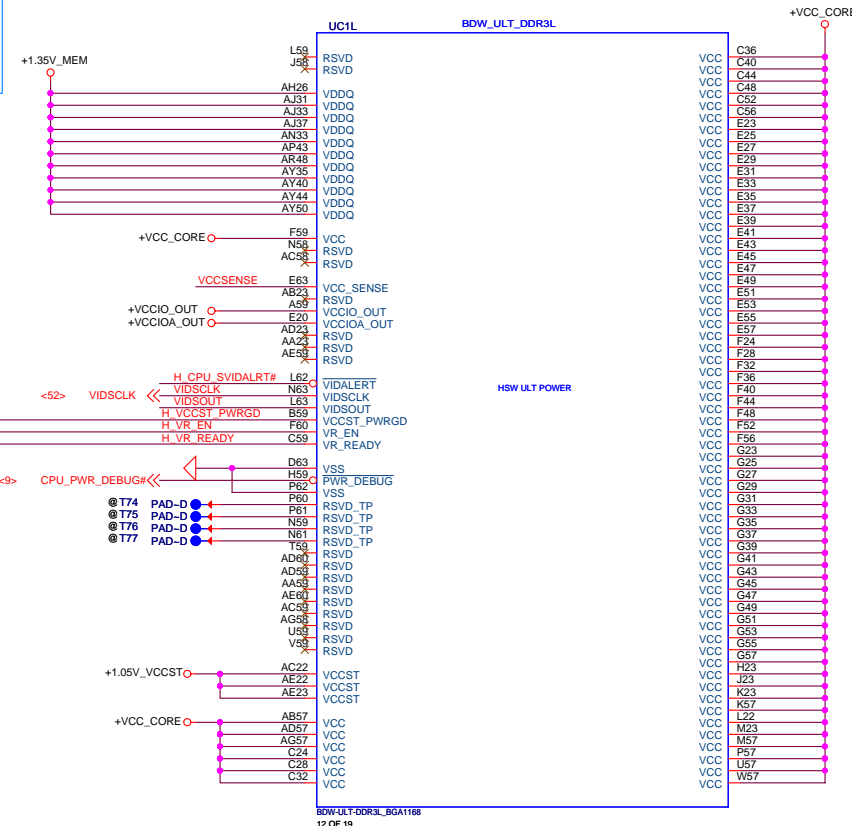
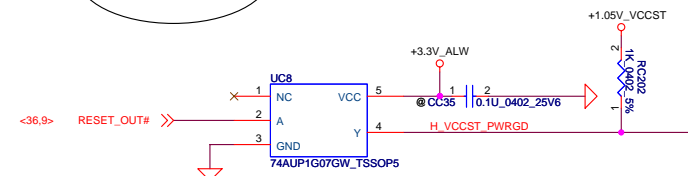
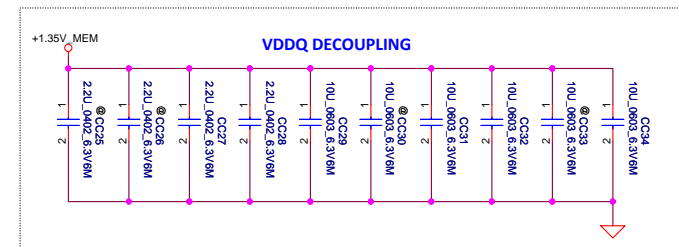
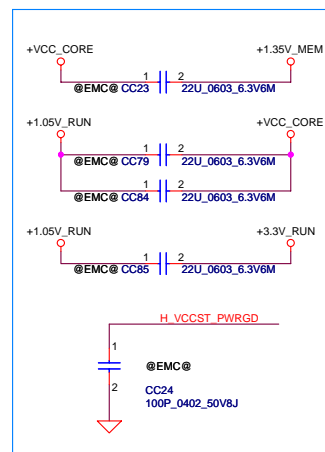
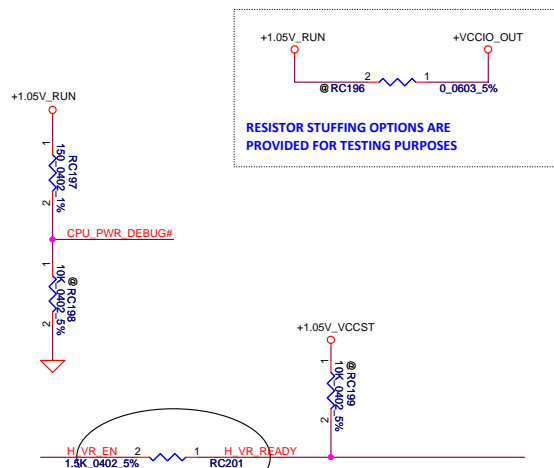
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## ESD Request



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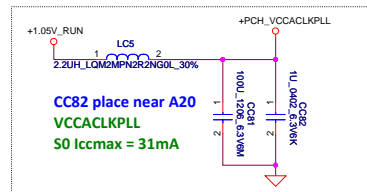
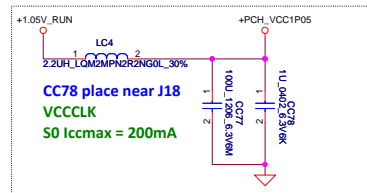
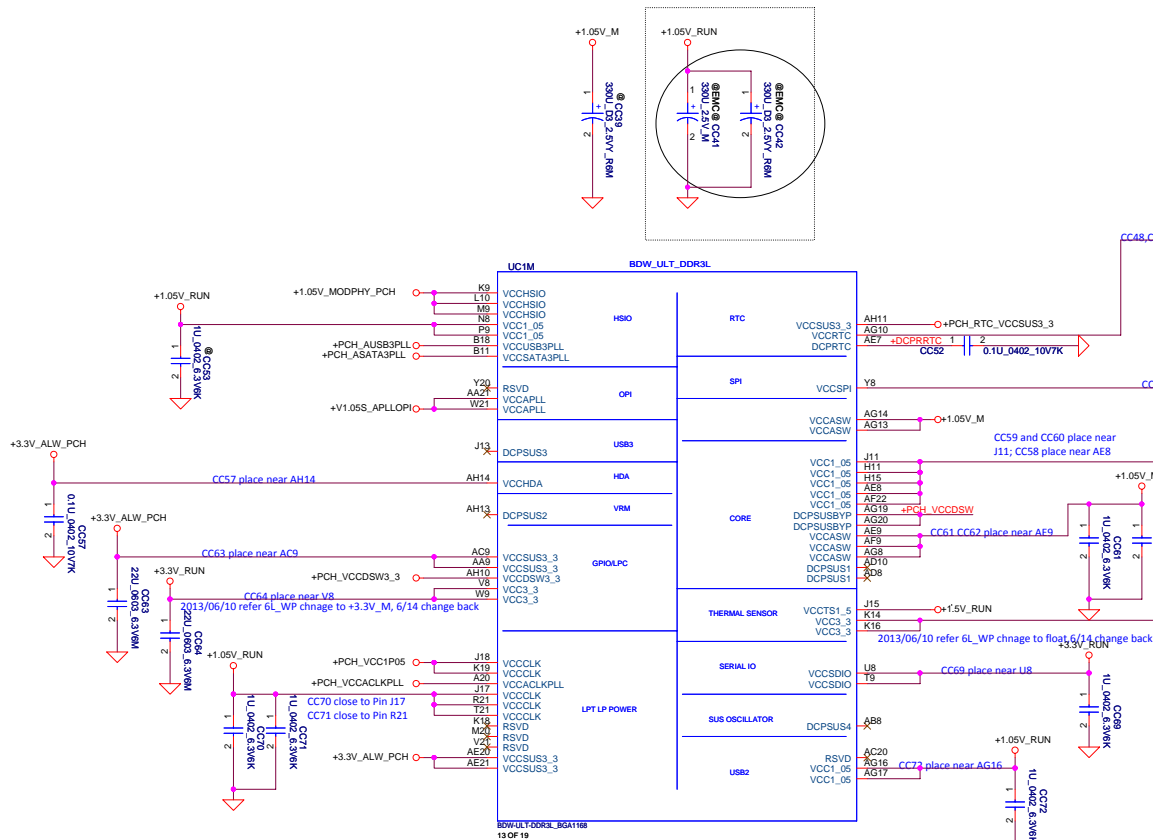
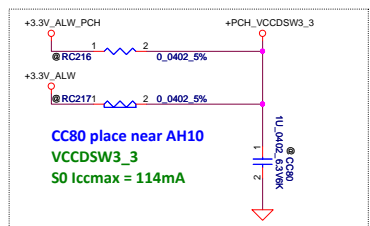
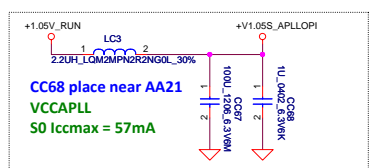
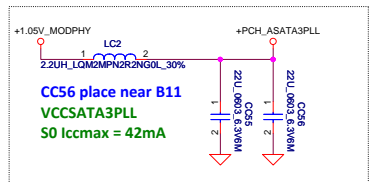
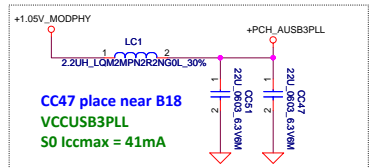
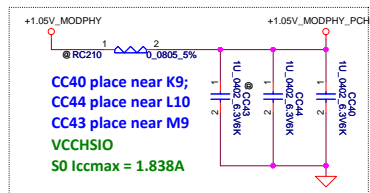
**SCHEMATICS,MB AA913**

**4019RA**

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Voltage Rail	Voltage (V)	S0 Iccmax Current (A) <sup>3</sup>	Sx Iccmax Current (A) <sup>3</sup>	Drop In Iccmax (A) <sup>3</sup>	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCDSW3_3	1.05	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCDSW3_3	3.3	0.017	0	0	0
VCCASW	1.05	0.458	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCHDA	3.3	0.011	~1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.003	0	0
DcpSus1*	1.05	0.109	0.014	0	0
DcpSus2*	1.05	0.023	0.001	0	0
DcpSus3*	1.05	0.010	0.001	0	0
DcpSus4*	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	~1 mA	~1 mA	~1 mA	See notes 1, 2



Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

#### Power Rail Isolation

Voltage Supply	Isolation (power rail isolation required)	PCH Pins sharing power rail
V1.05s	Core	T11, H11, H15, A15, A17, A21, W21
	OPT	A21, W21
	HSD	V1, L15, N1, P1, B11, B15, W1
	INP	N15, A17, A21
	CLUPLL	A20
	CLU(A)	B21, Y21
	CLU(B)	T11, K19
	CLU(C)	T17
V3.3s	SPD	A15, A17, A21, A23, A25
	RTC	A11
	HDA	A11, A13
V3.3s	SPD	V1, W1
	SPD	V1, T1
	Thermal Sensor	K14, K15

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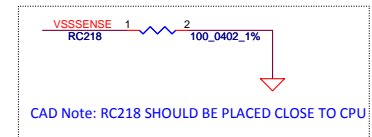
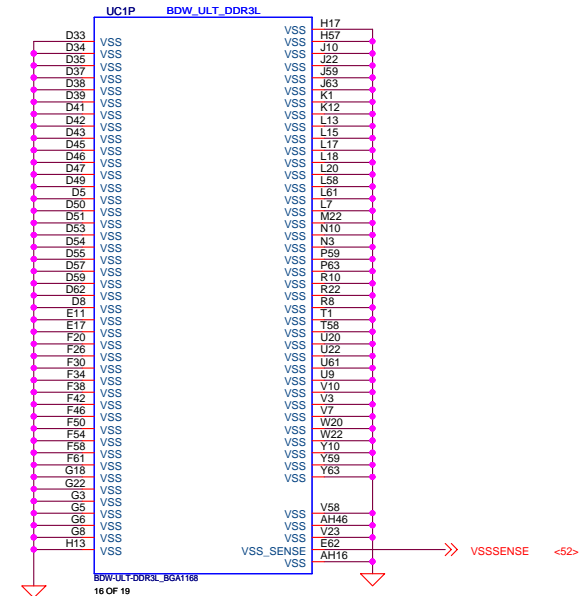
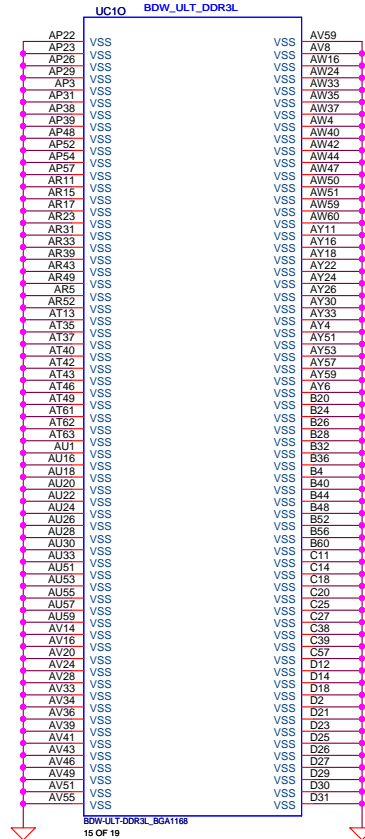
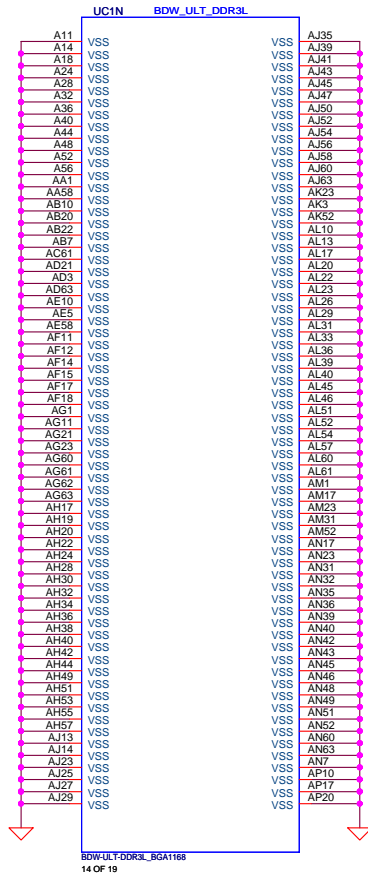
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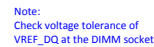
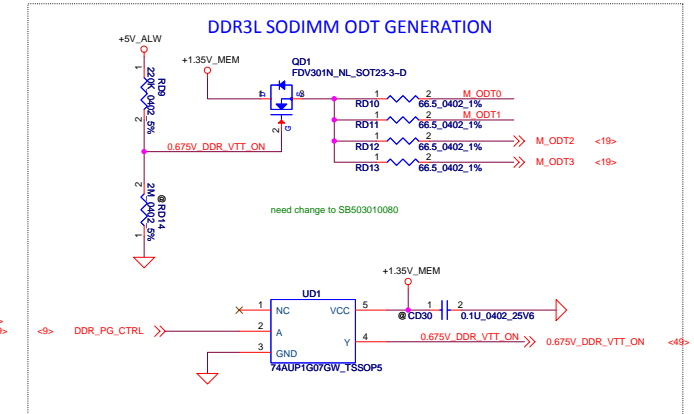
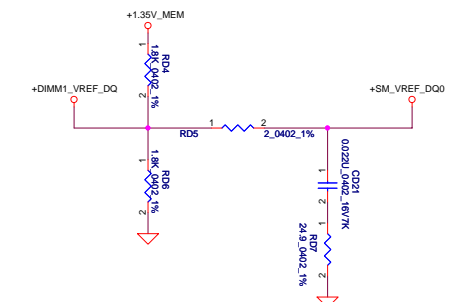
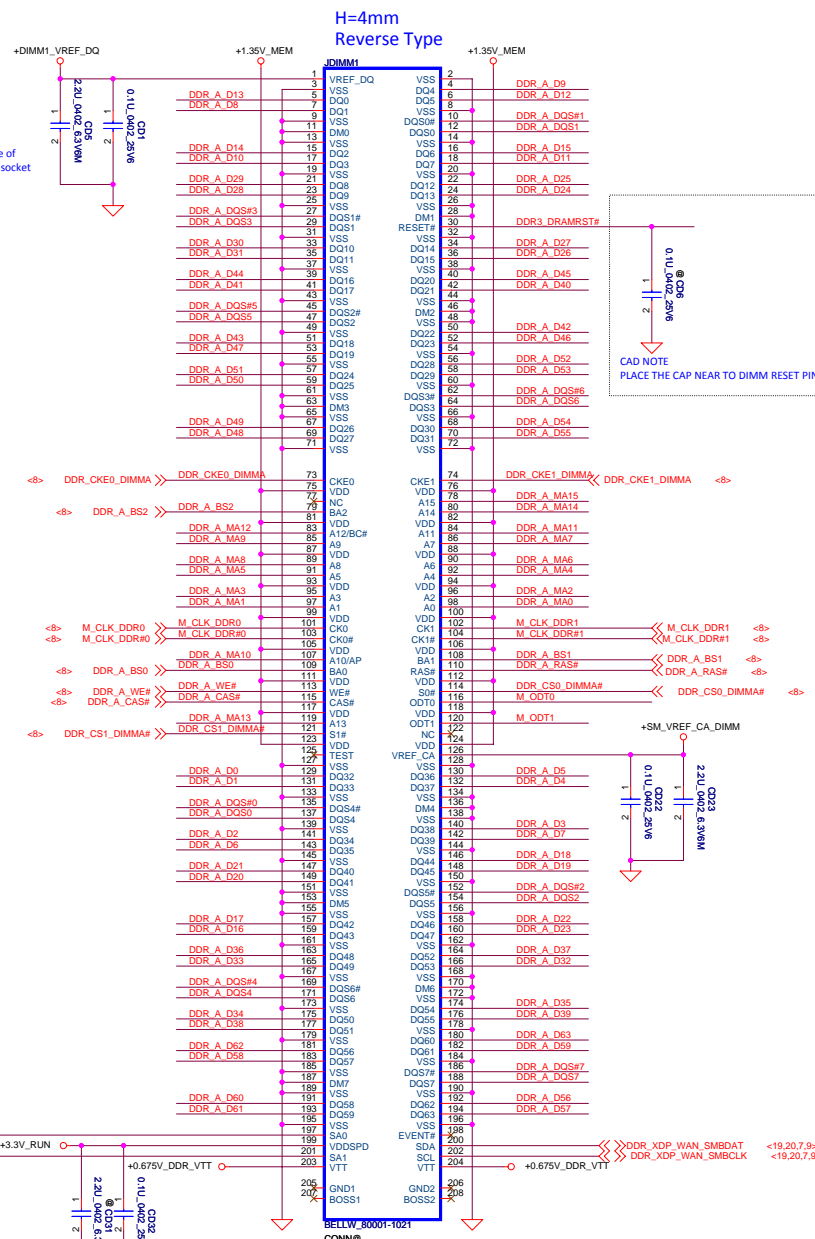
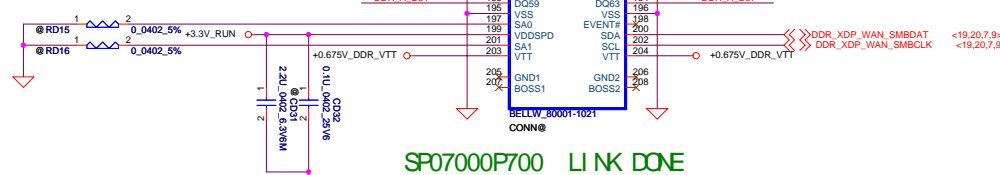
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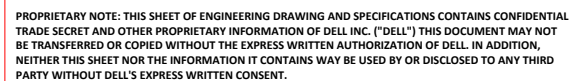
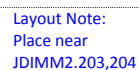
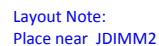
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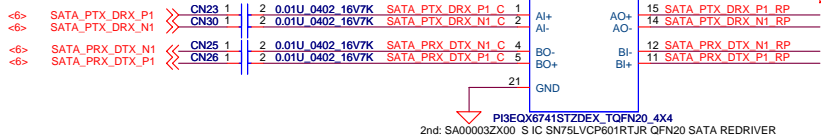
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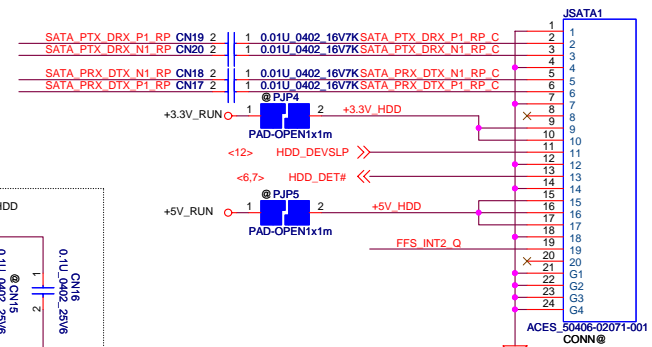
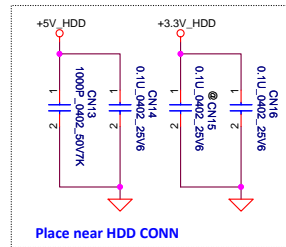
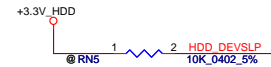
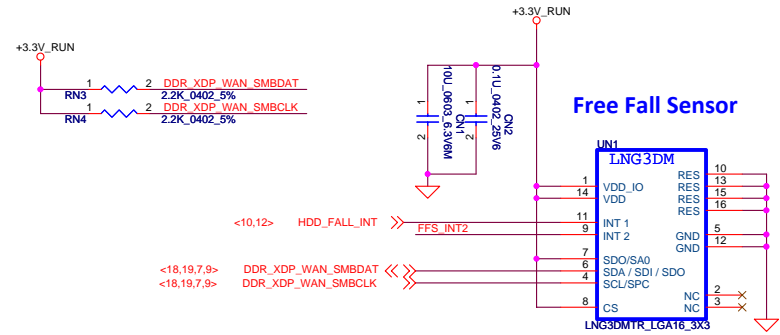
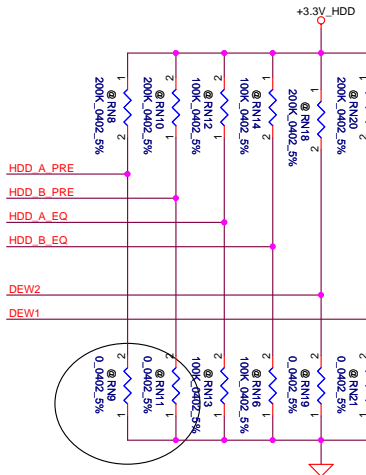
1

## SATA Repeater



PERICOM PI3EQX6741ST:  
Pin6/16, NC  
Pin8/9, Pre-emphasis

TI SN75LVCP601RTJR  
Pin6/16, de-emphasis width setup  
Pin8/9, de-emphasis



SP010016L00 LINK DONE

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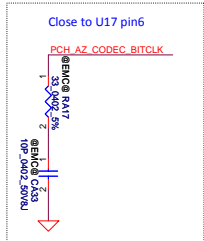
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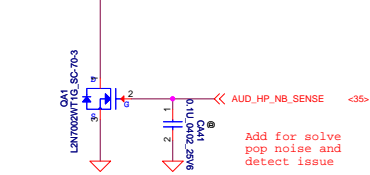
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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

40 mils trace keep 20 mil spacing

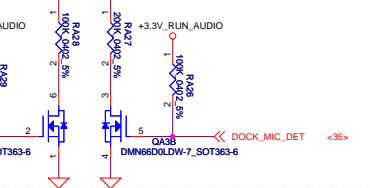


Place closely to Pin 13. AUD\_SENS



AUD\_SENSE\_B

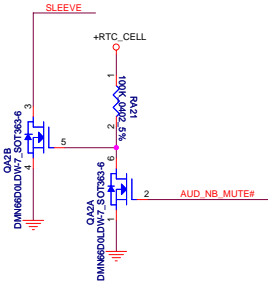
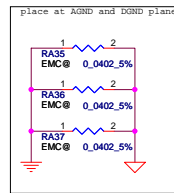
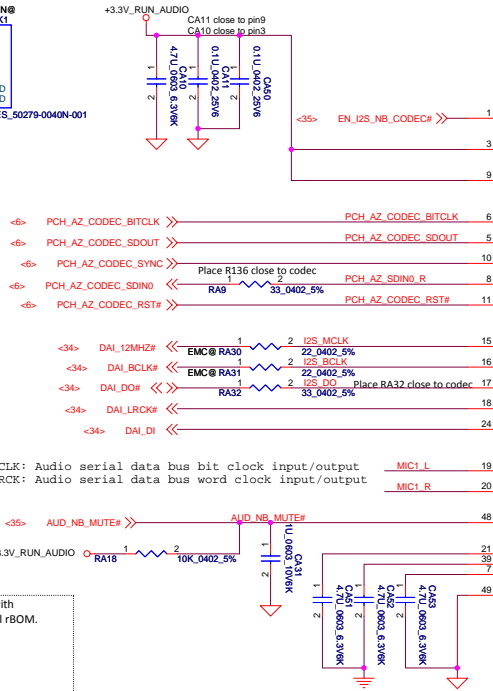
1 RA38 2 100K\_0402\_5% +3.3V\_RUN\_AUDIO



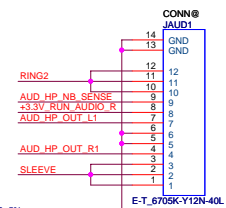
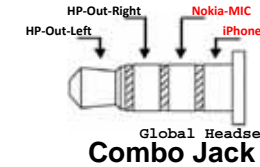
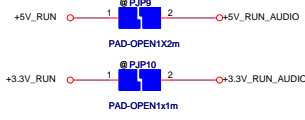
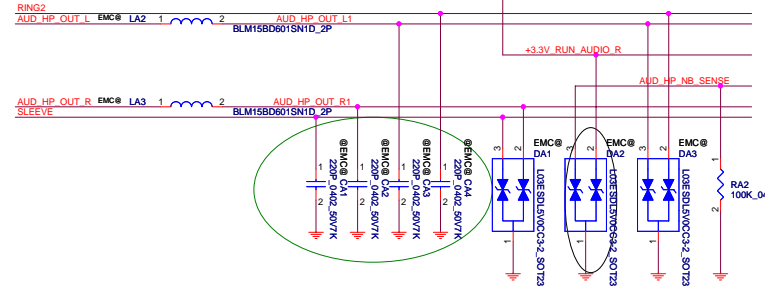
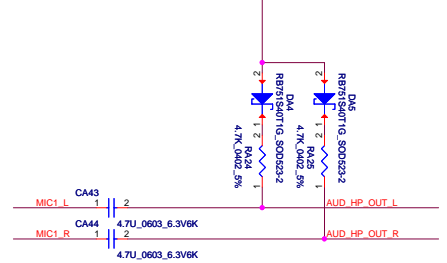
The schematic diagram shows the MIC1 module with the following connections:

- Pin 1: GND
- Pin 2: VCC
- Pin 3: GND
- Pin 4: DMIC1\_CLK1
- Pin 5: +3.3V\_RUN
- Pin 6: DMIC1

The module is labeled MIC1 and SPM1437HM4H-6\_BP.



PCB layout for the HP-MIC1 (JDU1) showing various signal and power connections. The diagram includes labels for components like capacitors (CA25, CA28, CA29, CA35, CA17, CA18), resistors (RA7, RAB, RA12, RA13), and connectors (JDU1). It also shows signal traces for AUD\_OUT\_L, AUD\_OUT\_R, INT\_SPK\_L+, INT\_SPK\_R+, AUD\_PC\_BEEP, DMIC\_CLK\_L, DMIC1, and SLEEP/RING2. Power connections include +VDDA\_PVDD, +5V\_RUN\_PVDD, +MIC1\_VREF\_OUT, and +MIC1\_VREF\_OUT. Ground connections are shown for GND, GND1, and GND2. The layout includes a note "Place CA29 close to Codec" and a note "DMIC\_CLK0".



6705K- Y12N- 40L LINK DONE

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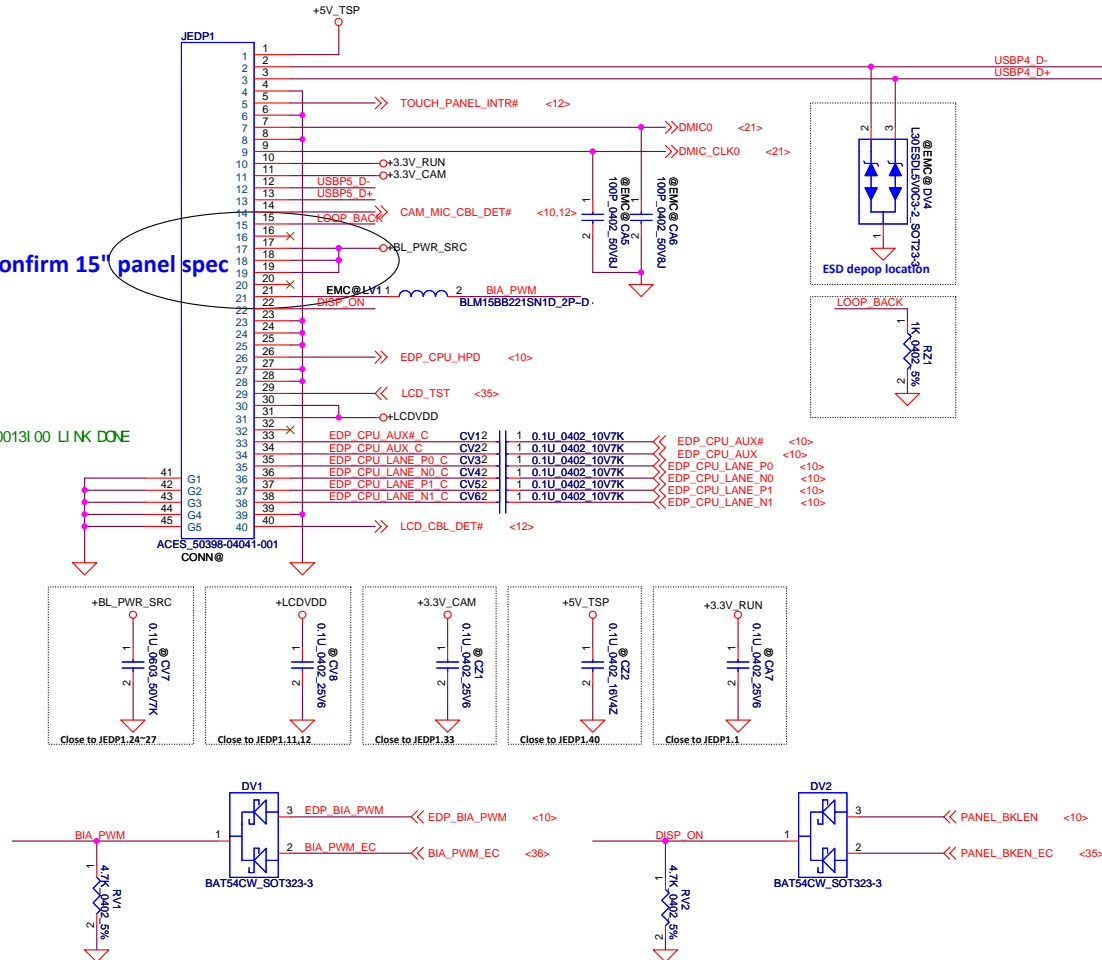
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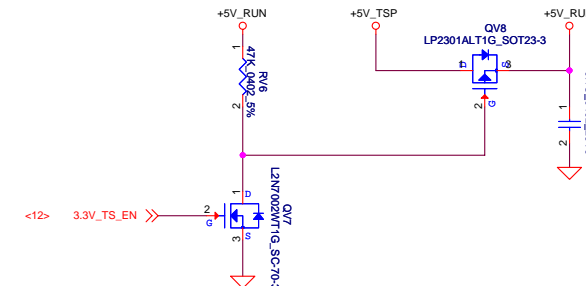


confirm 15" panel spec

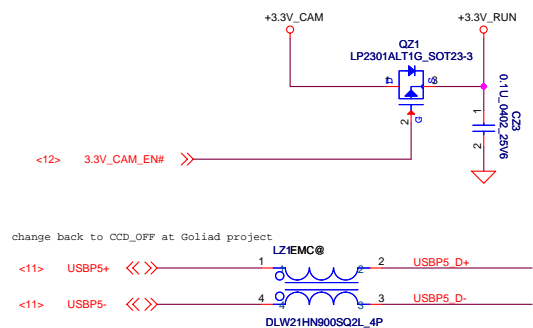
SP010013100 LINK DONE



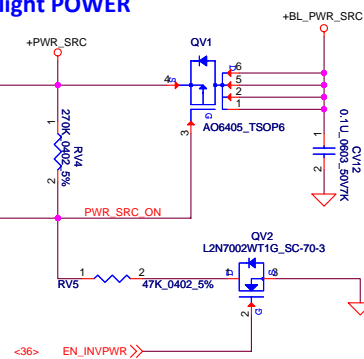
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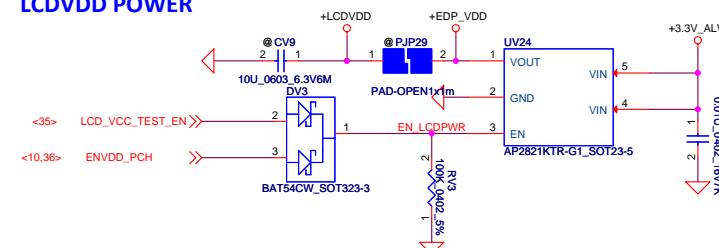
### WebCAM



### Backlight POWER



### LCDVDD POWER



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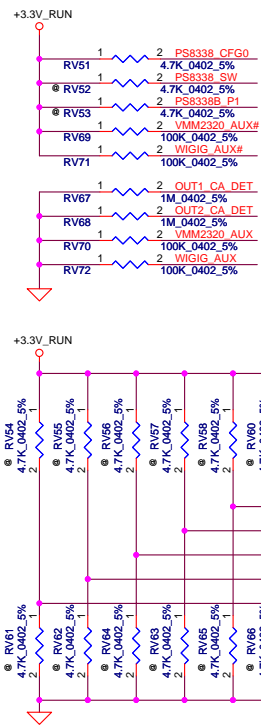






12" use 8339  
14"/15" use 8338 at DOCK config  
14"/15" use 12412 at Entry config

PCB	DP SWITCH
H12 UMA	PS8339+DP12412
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	DP12412
H14U_En	DP12412
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	DP12412
H15U_En	DP12412



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<10> DDI2\_LANE\_N0  
<10> DDI2\_LANE\_P1  
<10> DDI2\_LANE\_N1  
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<10> DDI2\_LANE\_N3

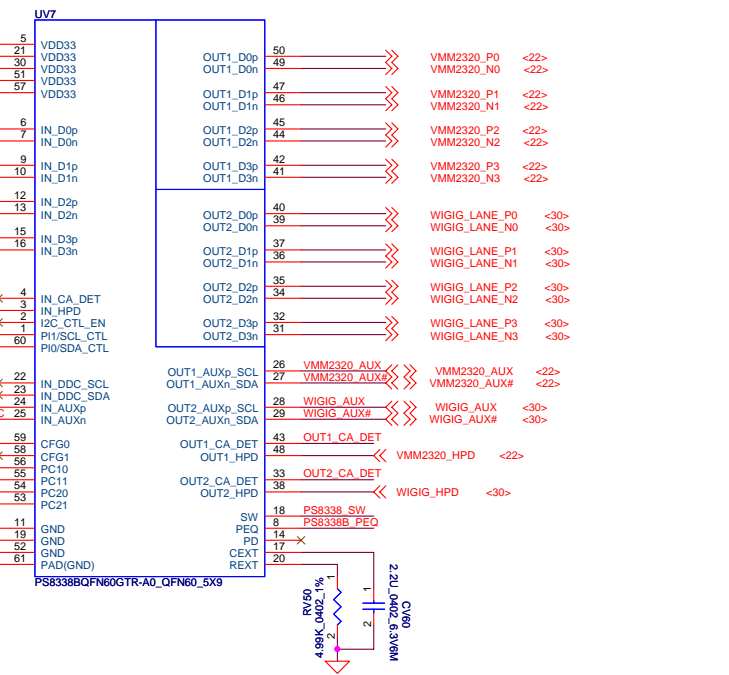
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<10> CPU\_DPC\_AUX#

CV62, CV69, CV70 close to pin30 &57  
CV66, CV69, CV70 close to pin5,21,51

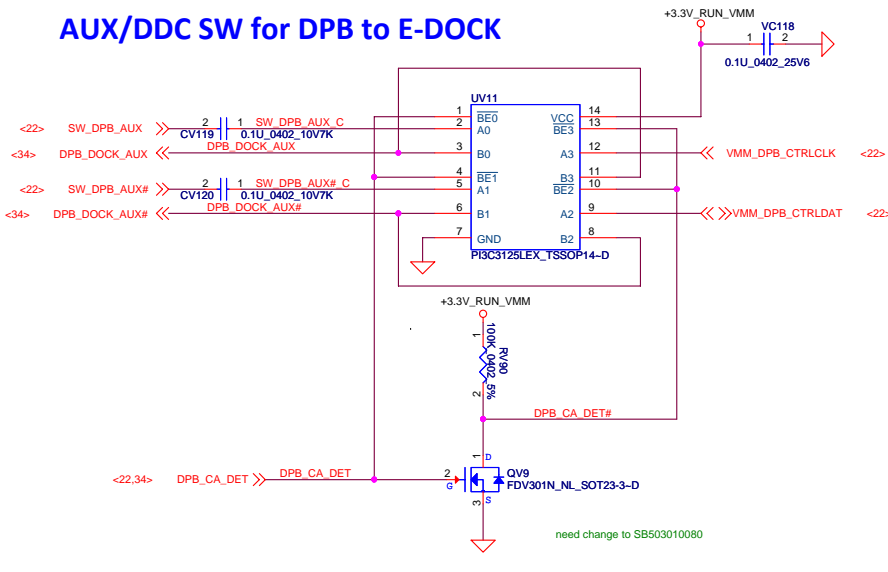
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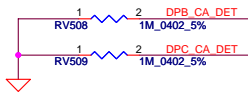
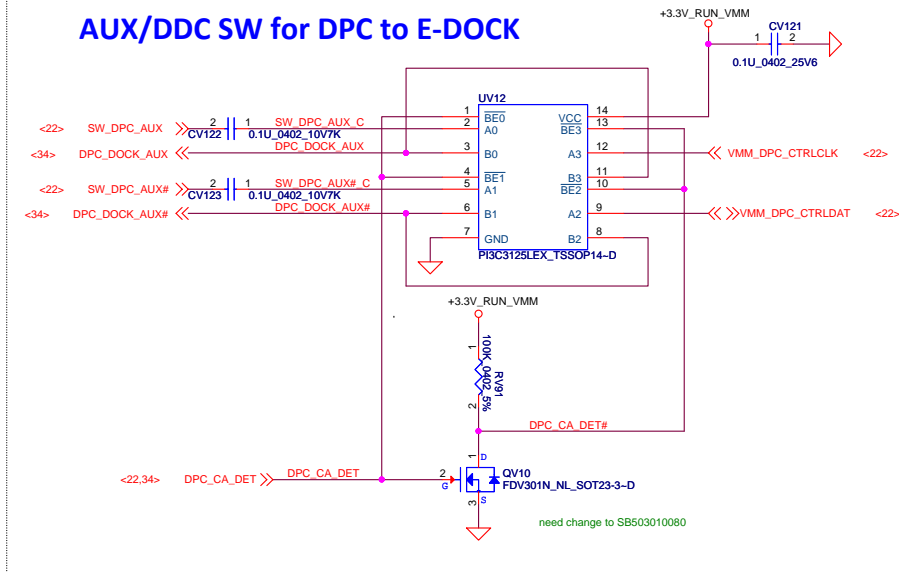
Dock has high priority when both ports plugged



## AUX/DDC SW for DPB to E-DOCK



## AUX/DDC SW for DPC to E-DOCK



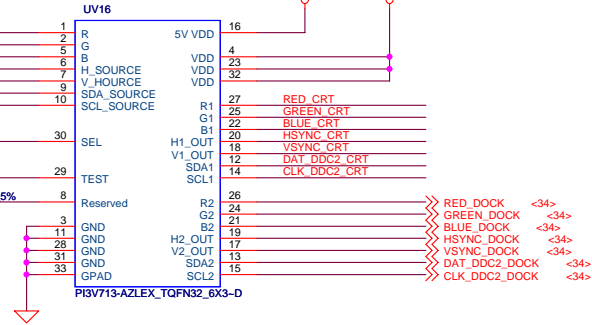
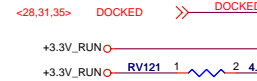
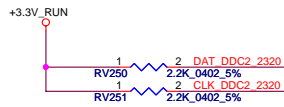
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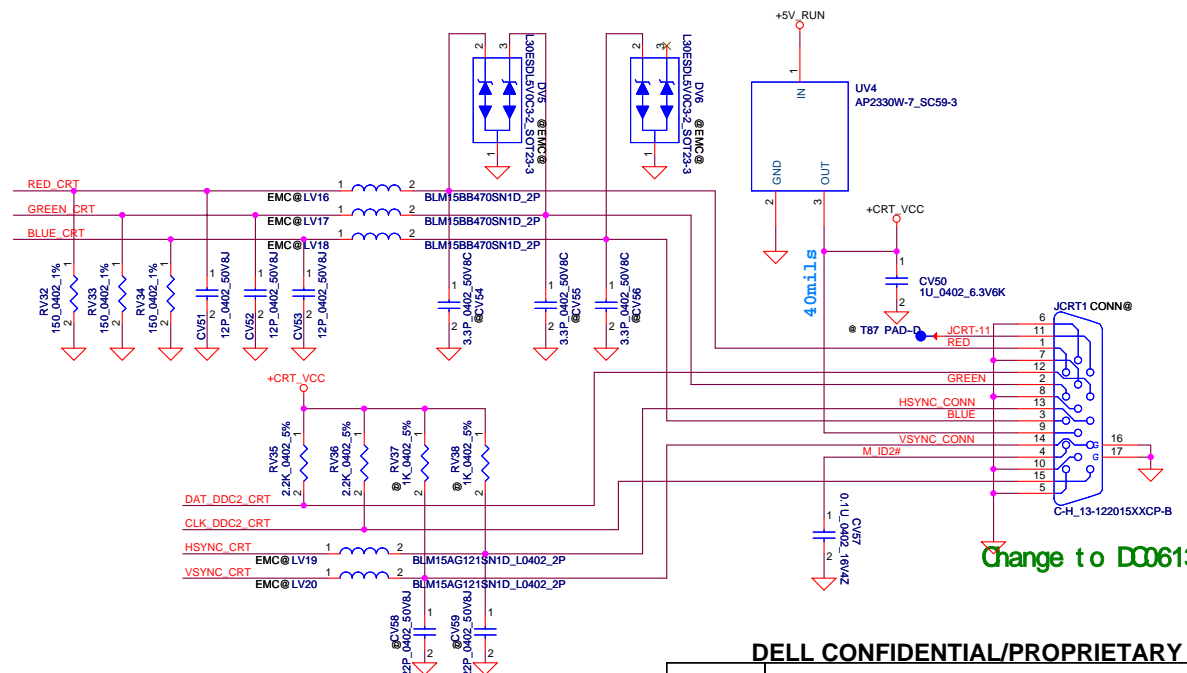
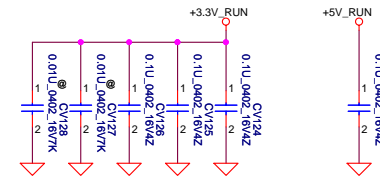
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source from VMM2320

PCB	VGA SWITCH
H12 UMA	NA
H12 Entry	NA
H14 DSC	PI3V713
H14 UMA	PI3V713
H14D_En	NA
H14U_En	NA
H15 DSC	PI3V713
H15 UMA	PI3V713
H15D_En	NA
H15U_En	NA



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SP1



Change to D0061307290.

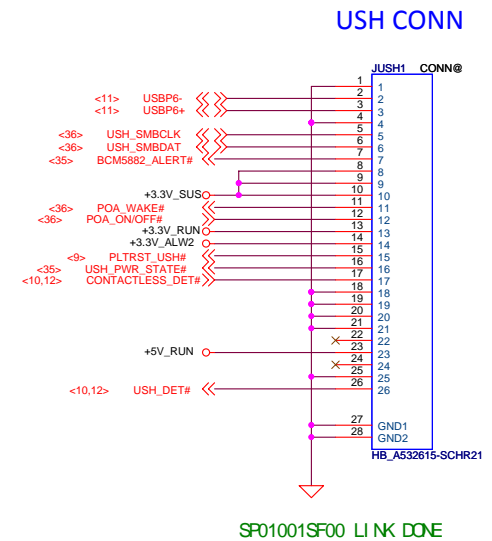
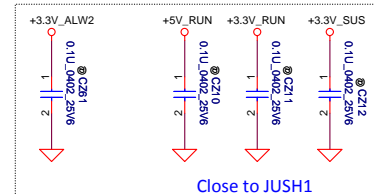
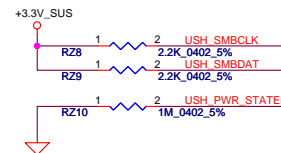
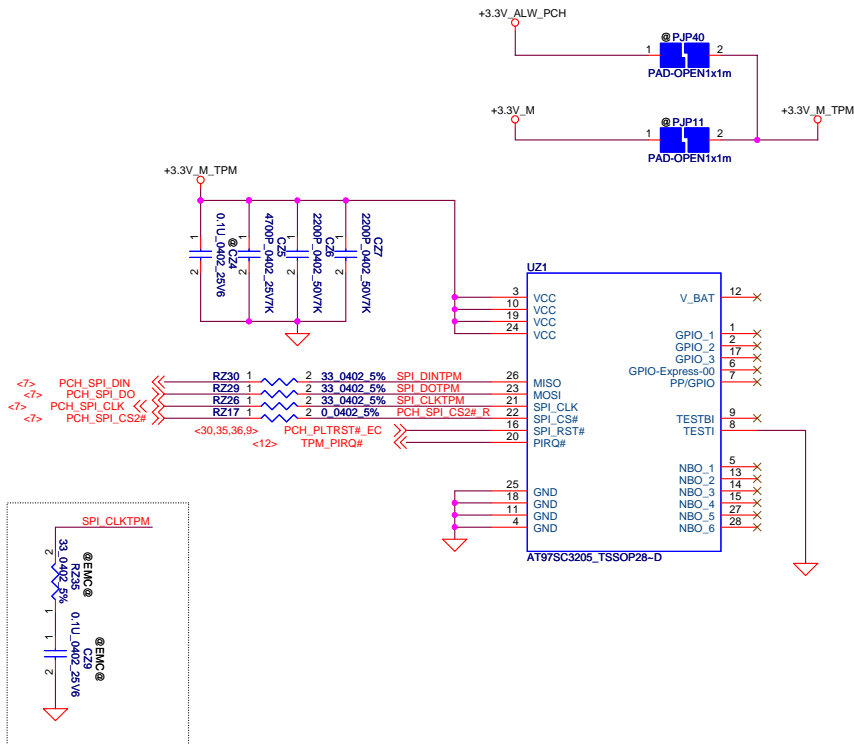


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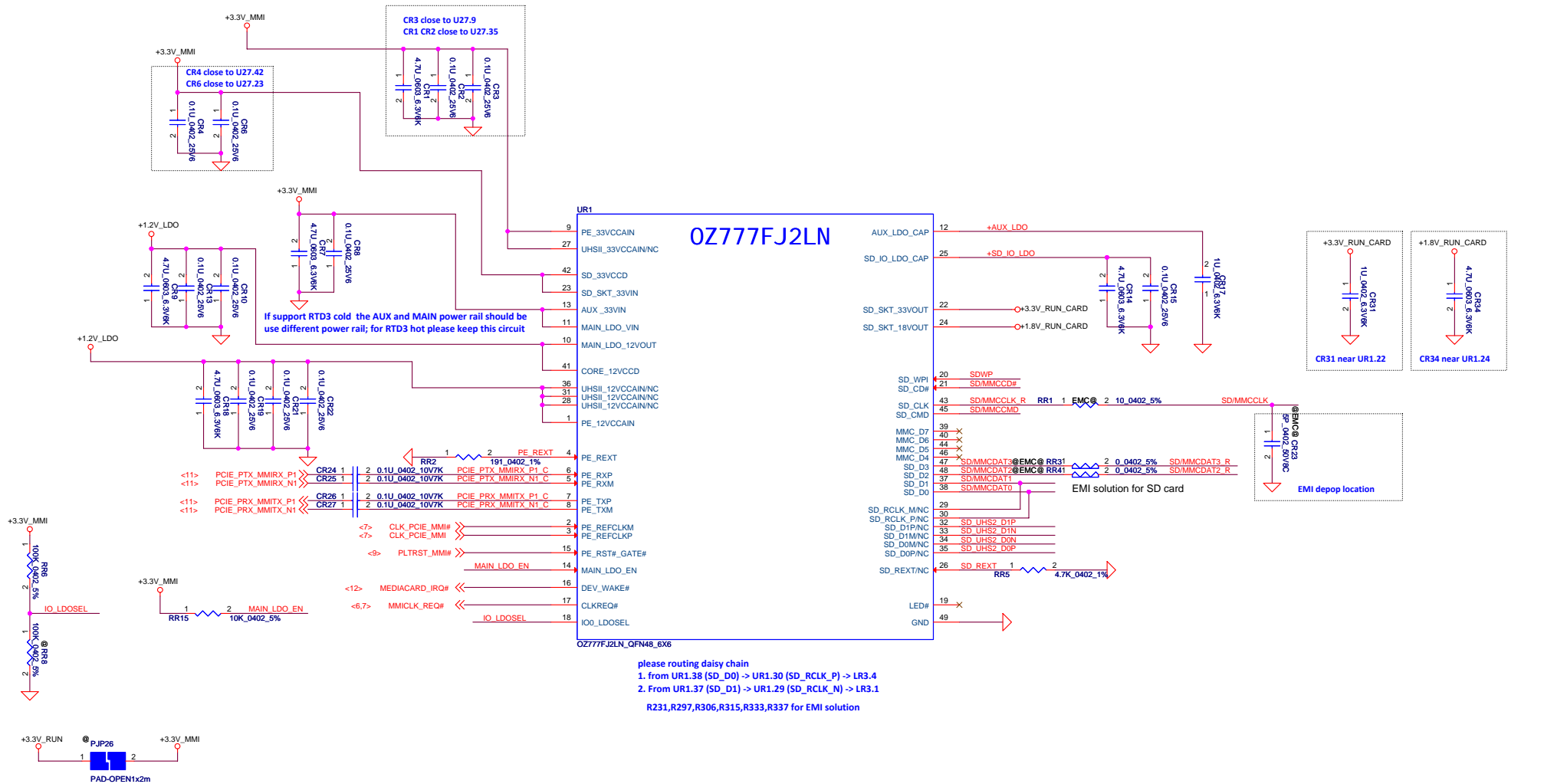
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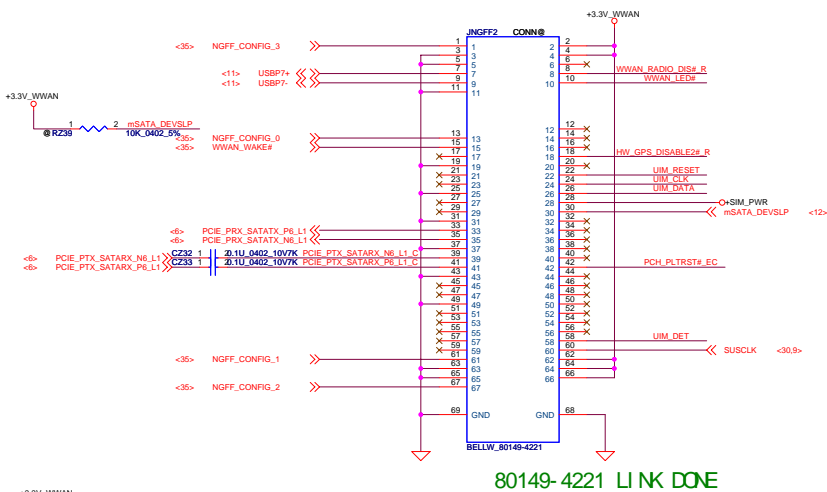




## NGFF slot B Key B

## NGFF for DSC

## NGFF slot A Key A

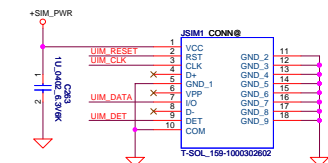


80149-4221 LINK DONE

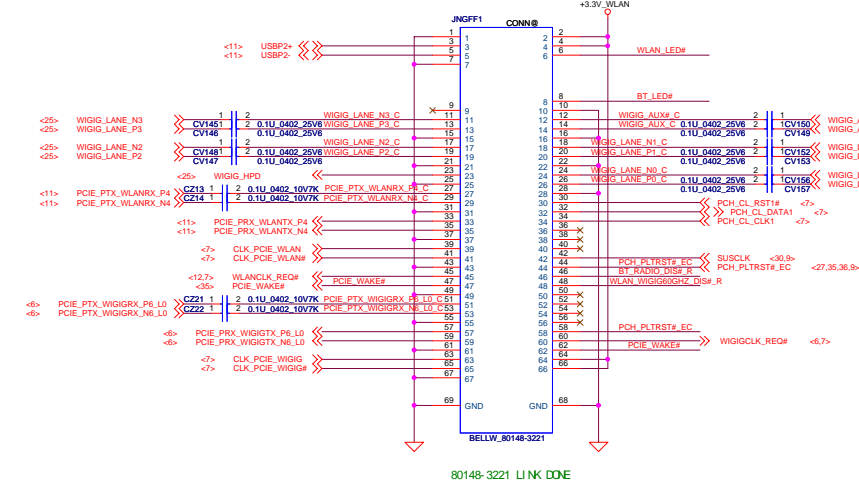
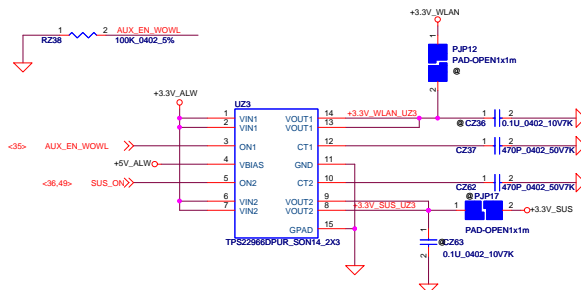


STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

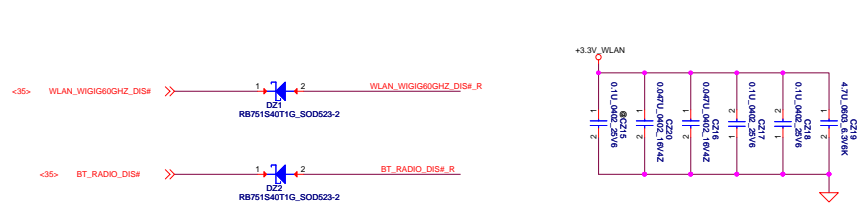
## SIM Card Push-Push



SP070011M00 LINK DONE



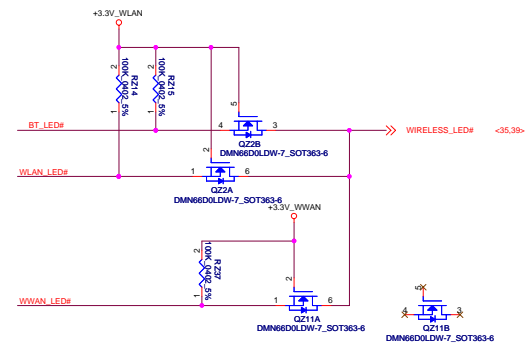
80148-3221 LINK DONE



## Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

## LED control circuit



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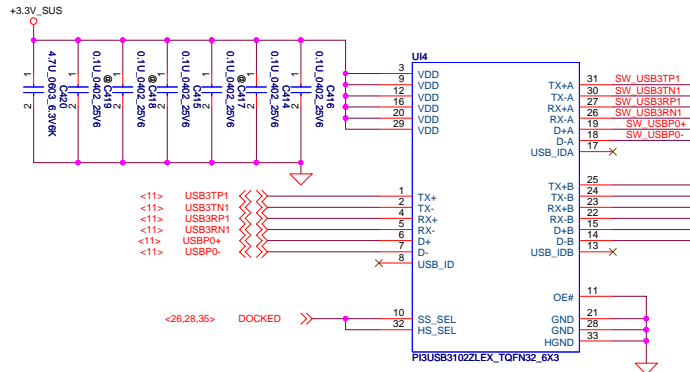
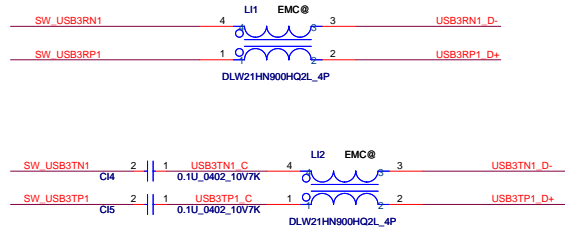
SCHEMATICS\_MB AA913

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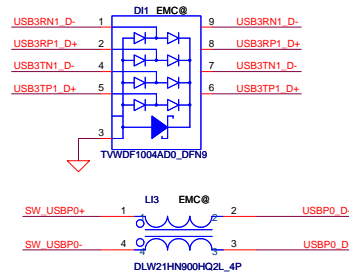
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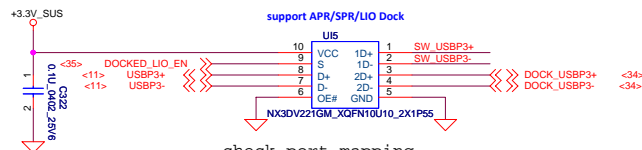
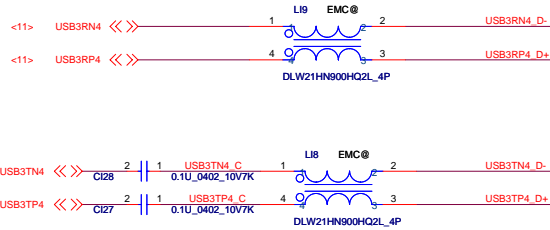
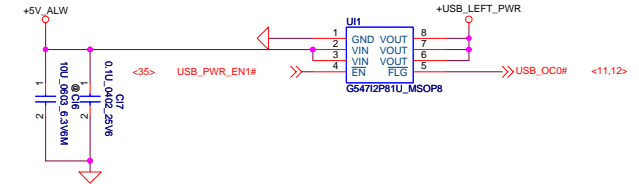
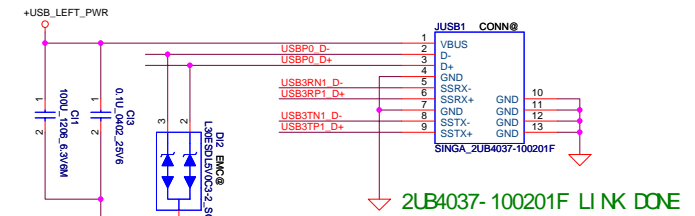


check port mapping

DOCKED	function
1	Dock
0	M/B

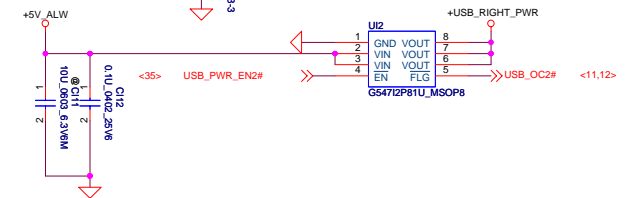
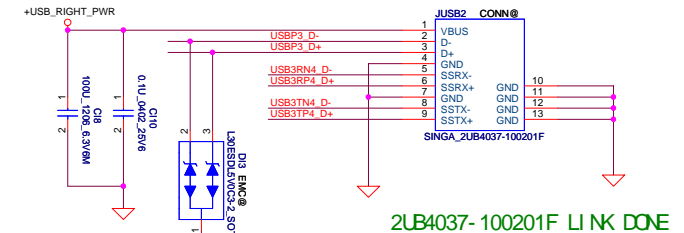
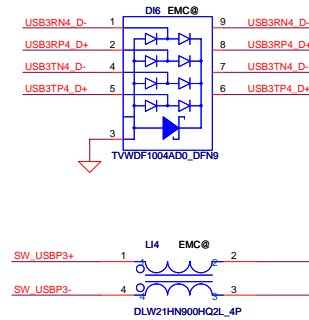


PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA



check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B



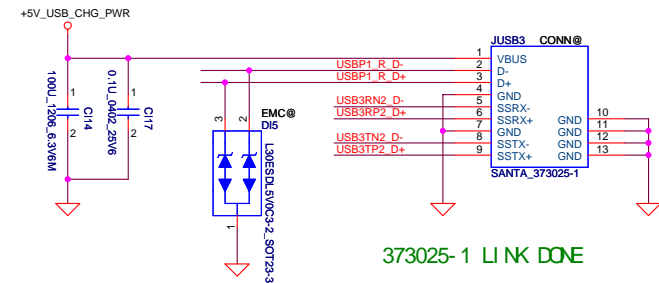
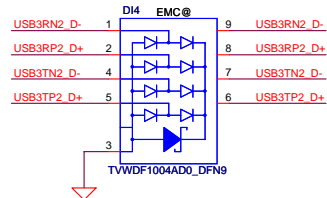
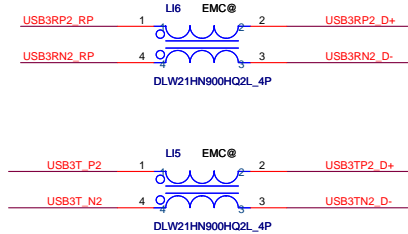
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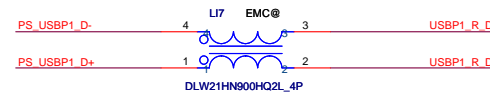
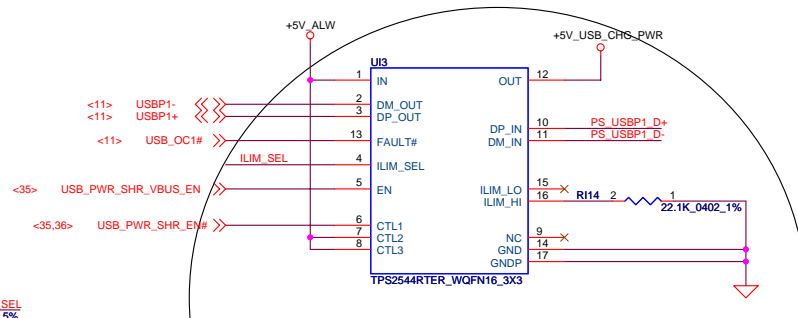


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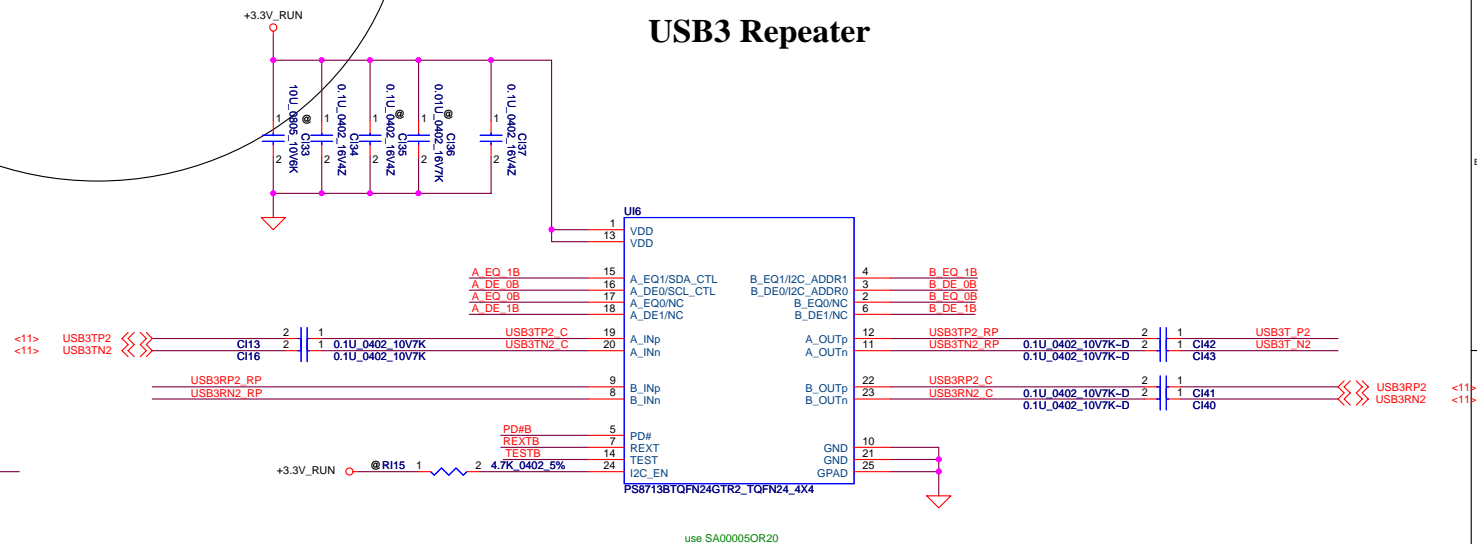
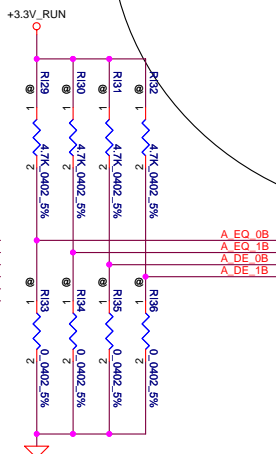
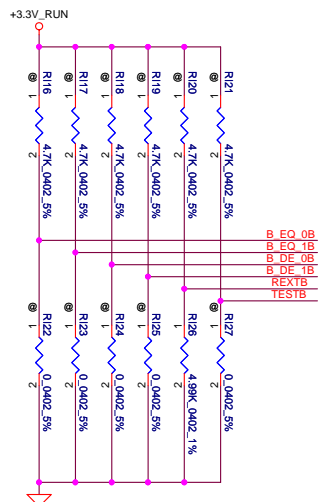
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373025-1 LINK DONE



## USB3 Repeater



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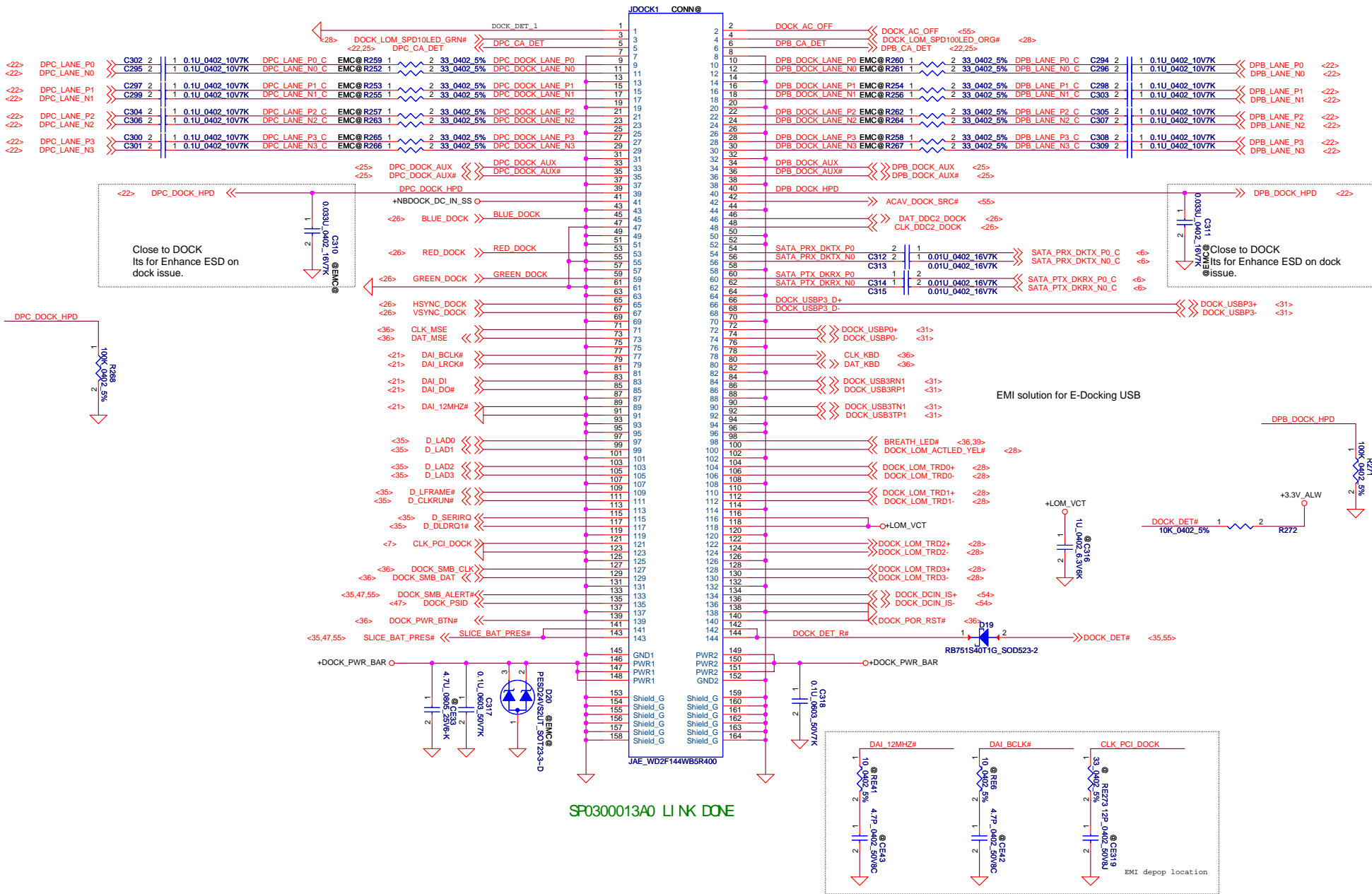
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Doesn't support.

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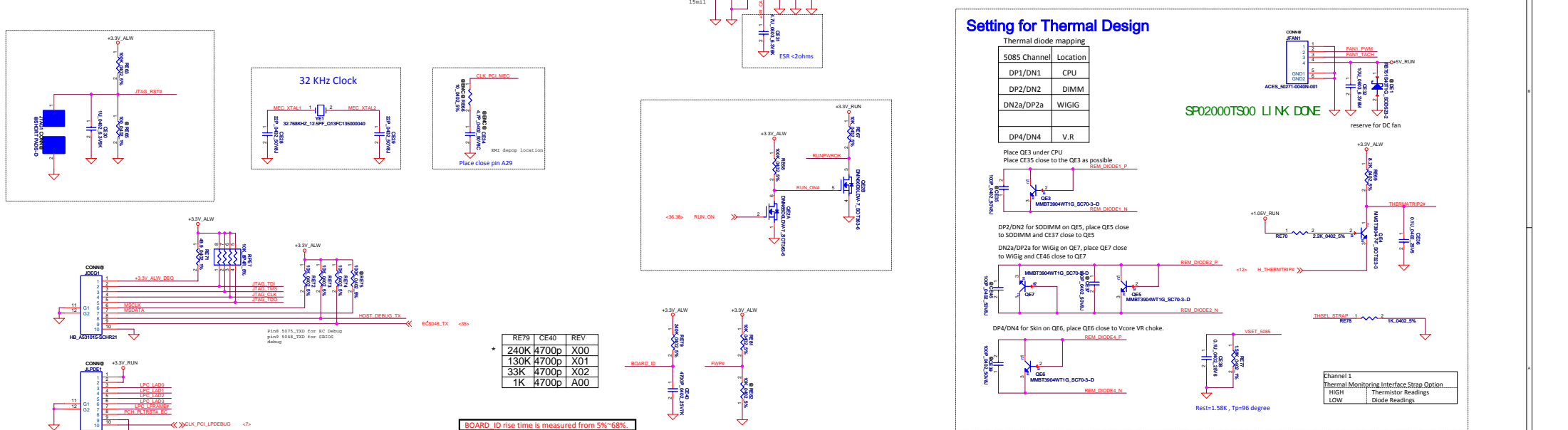
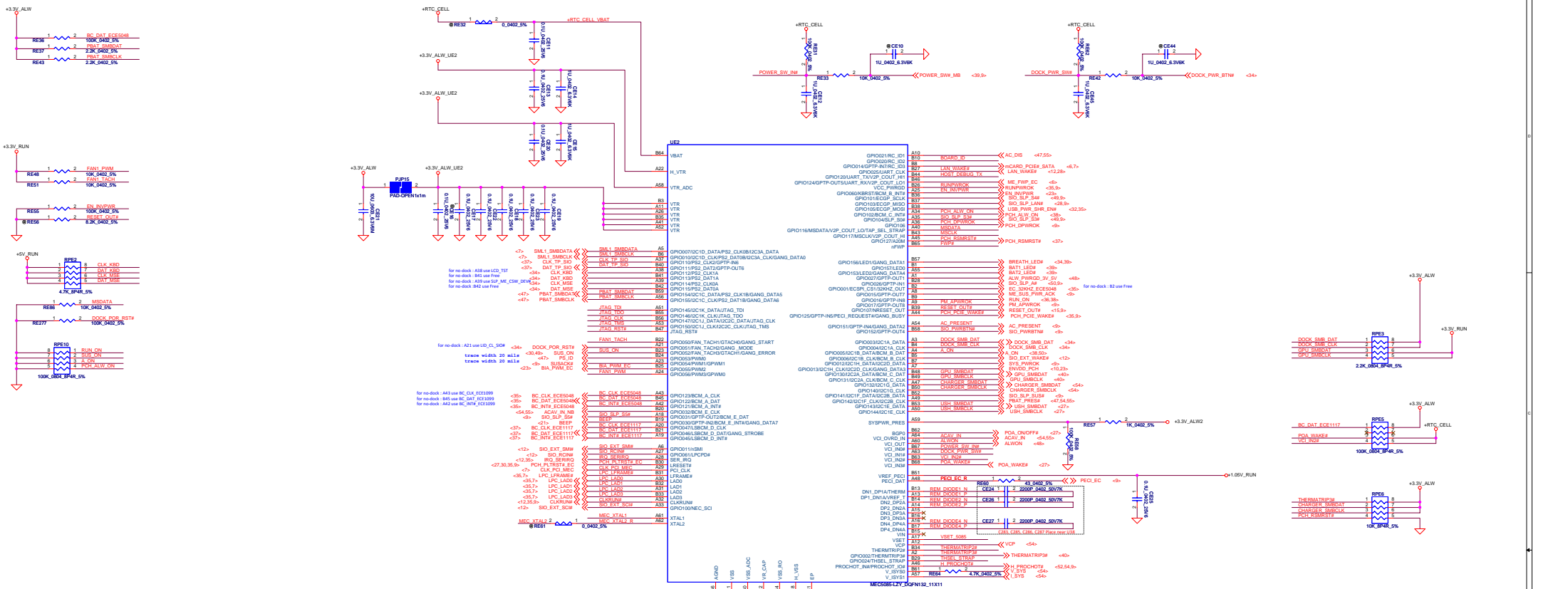
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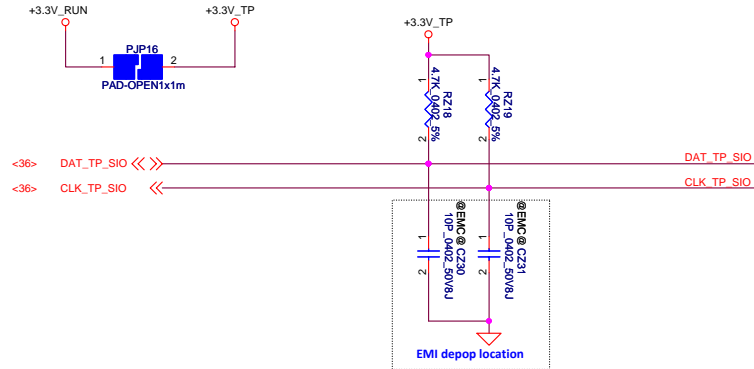
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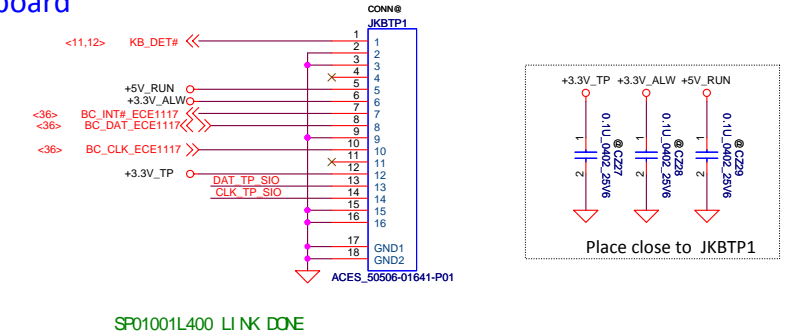




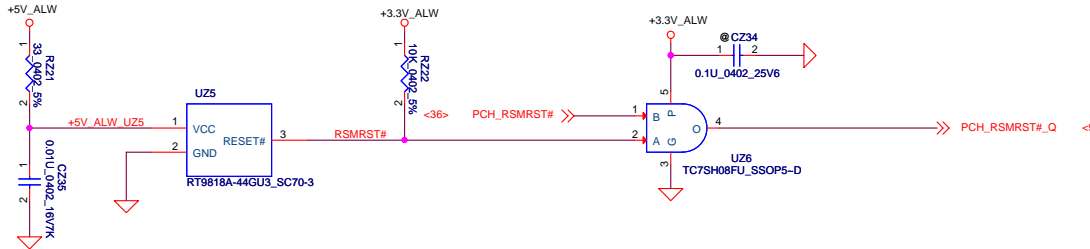
## Touch Pad



## Keyboard



## RSMRST circuit



### @eDP Cable

Part Number	Description
DC02C007A00	H-CONN SET 13M MB-EDP

### @eDP Cable w camera

Part Number	Description
DC02C007900	H-CONN SET 13M MB-EDP-CAMERA

### @eDP TS Cable w camera

Part Number	Description
DC02C007800	H-CONN SET 13M MB-EDP-CAMERA-TS

### @SATA Cable-Spindle HDD

Part Number	Description
DC02C007800	H-CONN SET 13M MB-SPINDLE HDD

### @SATA Cable-mSATA

Part Number	Description
DC02C007700	H-CONN SET 13M MB-mSATA HDD

### @DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

### @RTC BATT

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

### @FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

### @KBTP FFC

Part Number	Description
NBX0001JH00	FFC 16P G P0.5 PAD=0.3 66.5MM MB-TP 13M

### @Audio Board FFC

Part Number	Description
NBX0001JP00	FFC 12P F P.5 PAD=.35 26.85MM MB-AUDIO/B

### @USH Board FFC

Part Number	Description
NBX0001JP00	FFC 26P G P0.5 PAD=0.3 58MM MB-USH/B 13M

### @LED Board FFC

Part Number	Description
NBX0001JM00	FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M

### @PWR Board FFC

Part Number	Description
NBX0001JL00	FFC 6P G P0.5 PAD=0.3 31MM MB-PWR/B 13M

### @FP FFC-Validity

Part Number	Description
NBX0001JN00	FFC 8P F P0.5 PAD=0.3 170MM USH/B-FP VALIDITY

### @FP FFC-TCS

Part Number	Description
NBX0001JO00	FFC 8P F P0.5 PAD=0.3 164.8MM USH/B-FP-TCS

### @Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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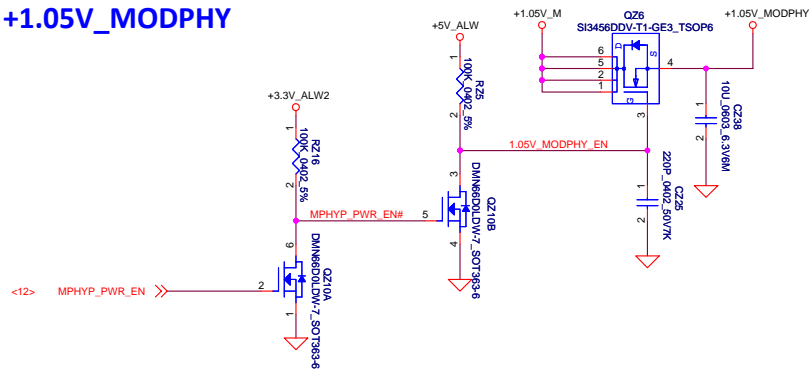
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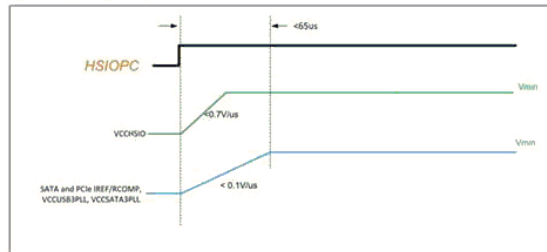
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## +1.05V\_MODPHY

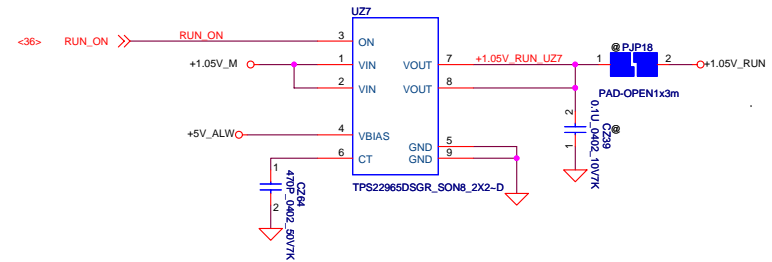


if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

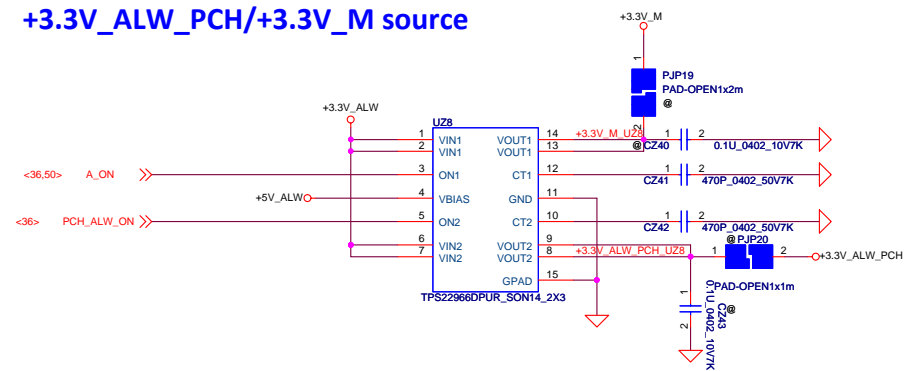
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



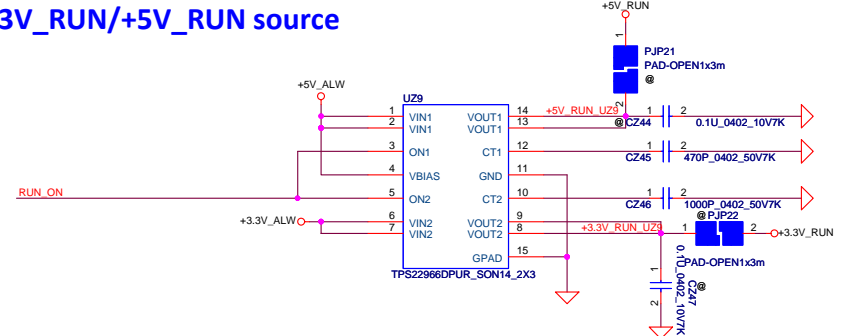
## +1.05V\_RUN source



## +3.3V\_ALW\_PCH/+3.3V\_M source



## +3.3V\_RUN/+5V\_RUN source



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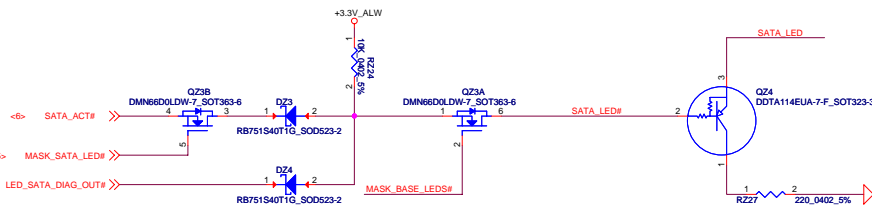
4019RA

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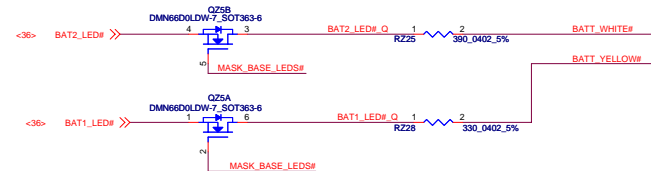
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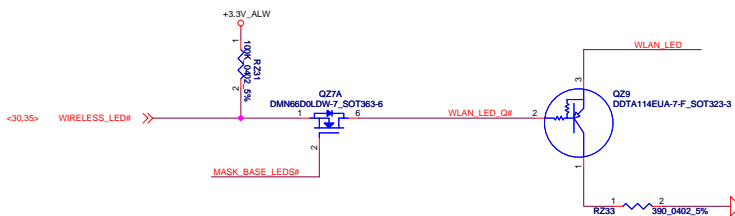
## HDD LED solution for White LED



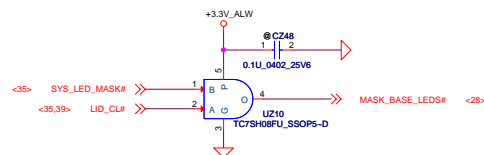
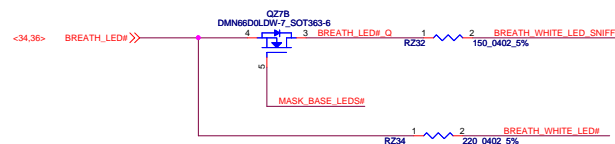
## Battery LED



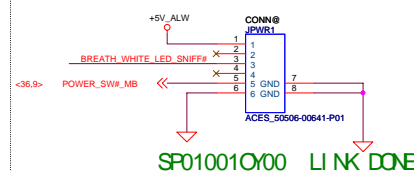
## WLAN LED solution for White LED



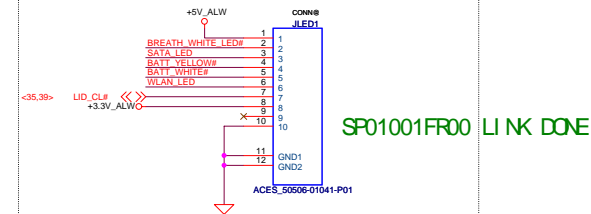
## Breath LED



## POWER board CONN



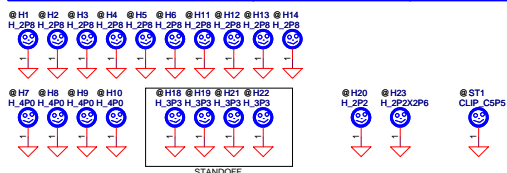
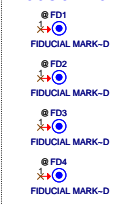
## LED board CONN



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

### Fiducial Mark



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I2CSlave Address

SMBUS_ALT_ADDR	Description
0	0x9E( Default )
1	0x9C( Multi - GPU usage)

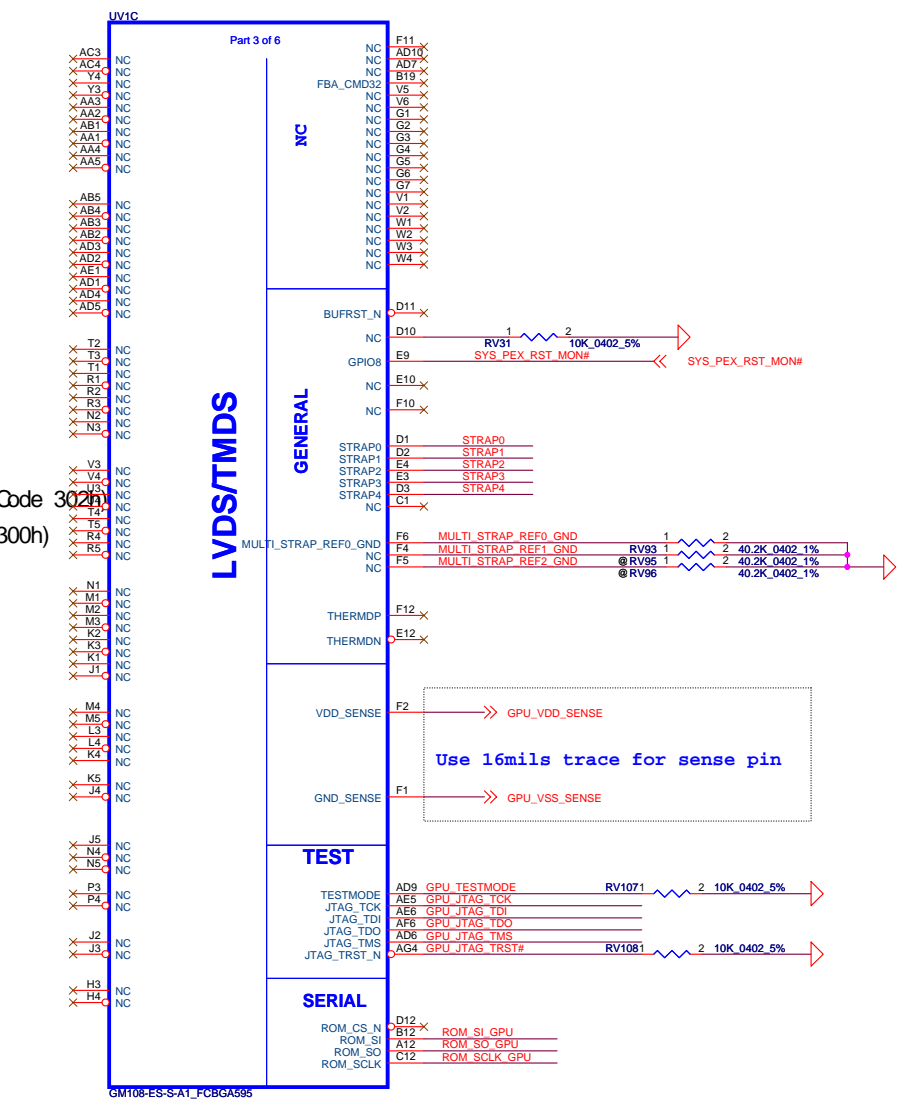
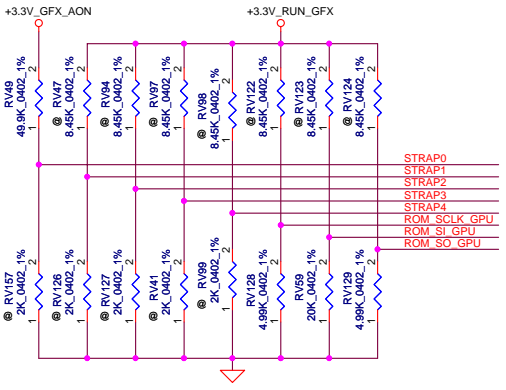
VGA\_DEVICE Setting

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device( Class Code 3020)
1	Primary Display or VGA Device( Class Code 300h)

Resistance Mapping to Hex Values

Resistor Value	Full-up to VDD3	Full-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

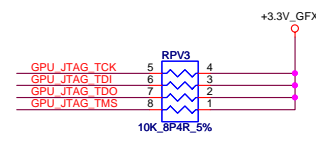
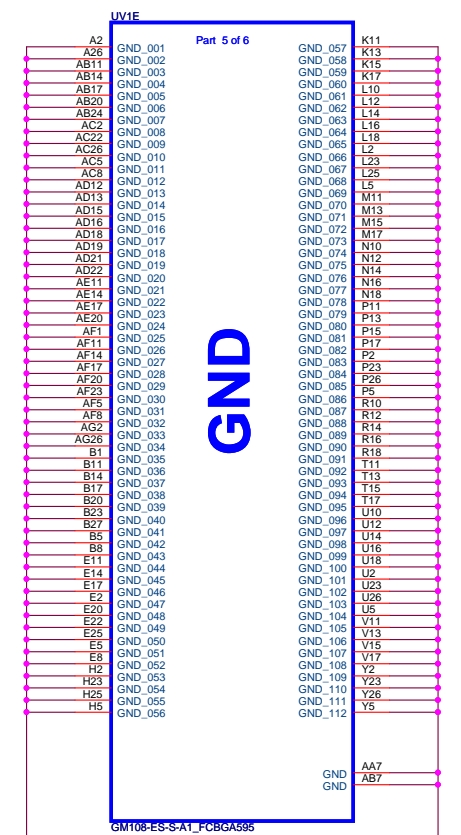
Decide ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down 20k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(default)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up			STRAP0 pull up 50k to +3.3V_GFX_AON	
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID\_SEL/PCIE\_CFG default set 0, need refer Platform Update Notification for the latest configuration

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VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x3	H5TC4G63AFR-11C	20k PD
Micron	0x4	MT41J256M16HA-093G:E	24.9k PD need change to MT41K256M16HA-107G:E
Samsung	0x5	K4W4G1646D-HC1A	30.1k PD

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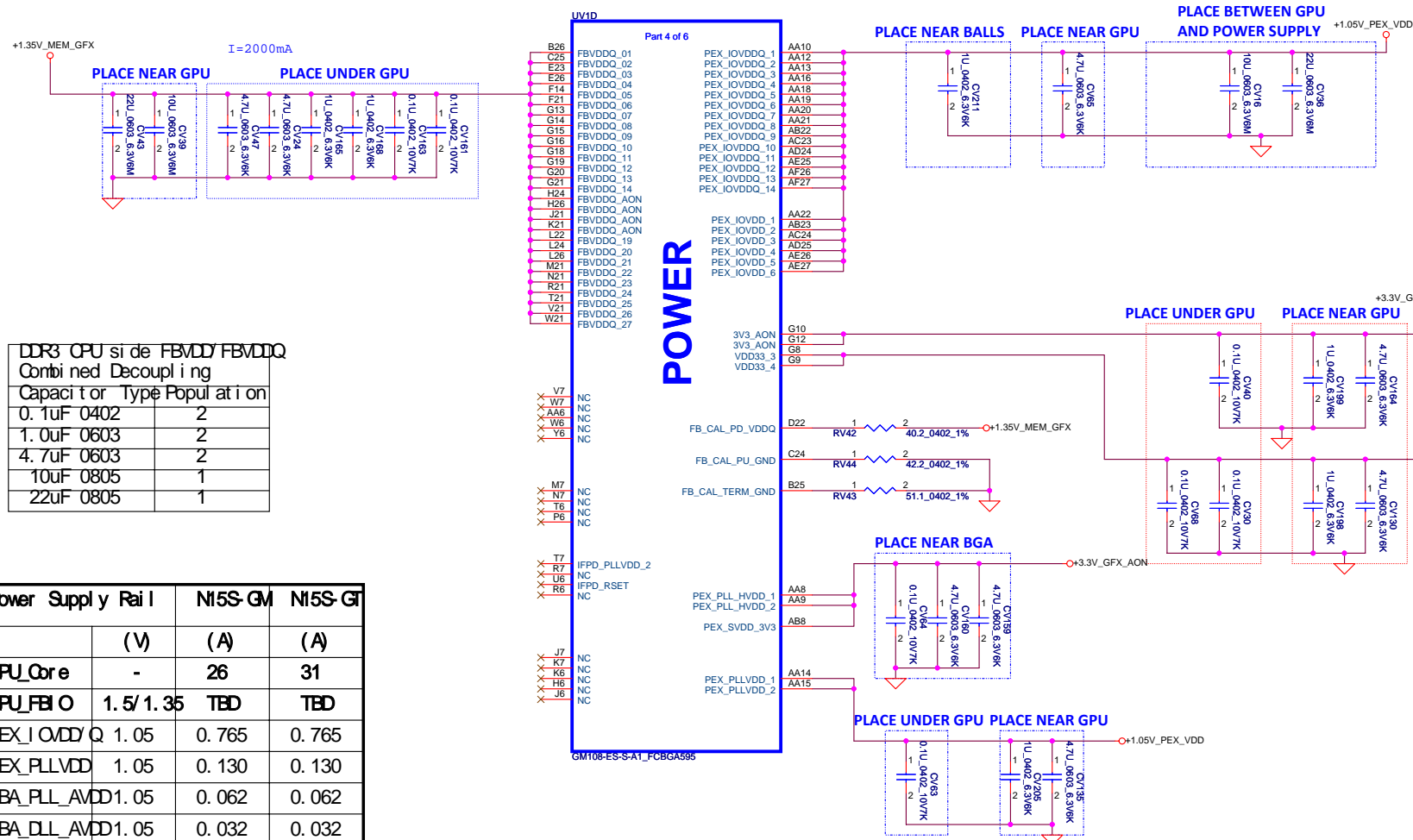
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DDR3 CPU si de FBVDD/FBVDDQ Conti ned Decoupli ng Capaci tor Type Popul at i on	
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	2
10uF 0805	1
22uF 0805	1

Power Supply Rail		Ni5S-GM	Ni5S-GM
	(V)	(A)	(A)
GPU_Core	-	26	31
GPU_FBI_O	1.5/1.35	TBD	TBD
PEX_I_OVDD_Q	1.05	0.765	0.765
PEX_PLLVDD	1.05	0.130	0.130
FBA_PLL_AVDD	1.05	0.062	0.062
FBA_DLL_AVDD	1.05	0.032	0.032
PLL_VDD	1.05	0.058	0.058
SP_PLLVDD	1.05	0.030	0.030
<b>1.05V Total</b>	<b>1.05</b>	<b>1.060</b>	<b>1.060</b>
VDD83+3V3AON	3.3	0.036	0.036
PEX_SVDD_3V3	3.3	0.167	0.167
PEX_PLL_HVDD	3.3	0.022	0.022
<b>3.3V Total</b>	<b>3.3</b>	<b>0.225</b>	<b>0.025</b>



Capacitor Type	Population
1uF 0402	1
4.7uF 0603	1
10uF 0805	1
22uF 0805	1

PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

Capacitor	Type	Population
0.1uF	0402	1
4.7uF	0603	2

Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

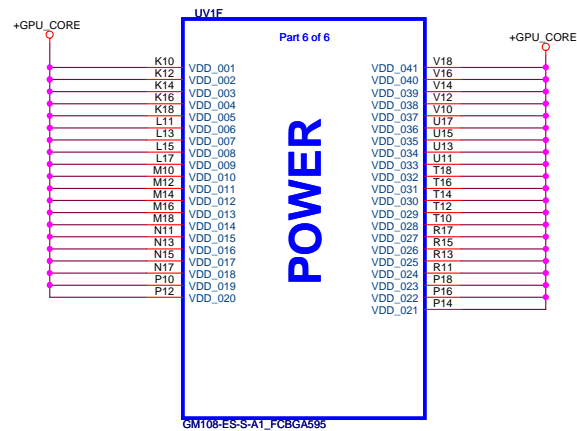
3V3_ACN Decoupling		
Capacitor	Type	Population
0.1uF	0402	1
1uF	0603	1
4.7uF	0603	1

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Caps on Power Side  
1UX4 4.7UX10 under GPU  
4.7UX5 22UX1 47UX2 330UX2 near GPU



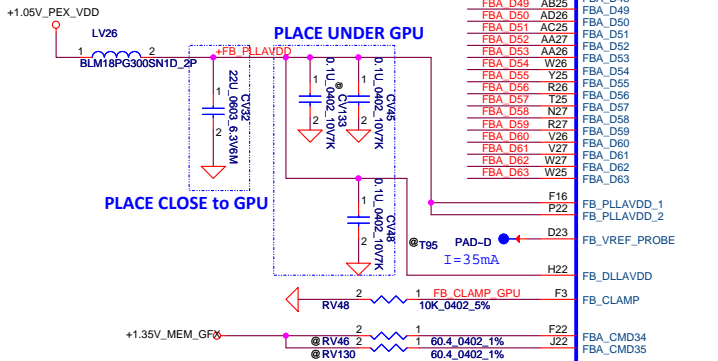
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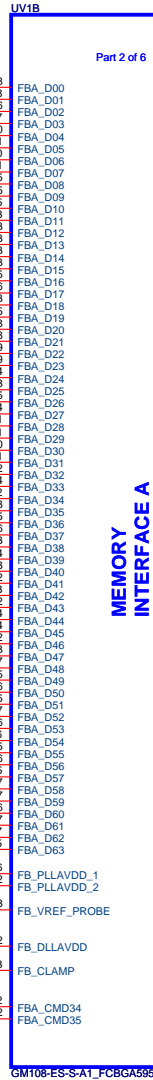
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# GDDR3L CMD Mapping Table

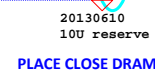
CMD0	CS0#	CMD32	
CMD1	ODT	CMD33	
CMD2	CKE	CMD34	
CMD3	RST	CMD35	
CMD4	A14	CMD36	A14
CMD5	RST	CMD37	RST
CMD6	A9	CMD38	A9
CMD7	A7	CMD39	A7
CMD8	A2	CMD40	A2
CMD9	A0	CMD41	A0
CMD10	A4	CMD42	A4
CMD11	A1	CMD43	A1
CMD12	BA0	CMD44	BA0
CMD13	WE#	CMD45	WE#
CMD14		CMD46	
CMD15	CAS#	CMD47	CAS#
CMD16		CMD48	CS0#
CMD17		CMD49	
CMD18		CMD50	ODT
CMD19		CMD51	CKE
CMD20	A13	CMD52	A13
CMD21	A8	CMD53	A8
CMD22	A6	CMD54	A6
CMD23	A11	CMD55	A11
CMD24	A5	CMD56	A5
CMD25	A3	CMD57	A3
CMD26	BA2	CMD58	BA2
CMD27	BA1	CMD59	BA1
CMD28	A12	CMD60	A12
CMD29	A10	CMD61	A10
CMD30	RAS#	CMD62	RAS#
CMD31		CMD63	



FBx PLL AVDD and FB DLL AVDD	
Capacitor Type Population	
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1



## 256x16 DDR3L

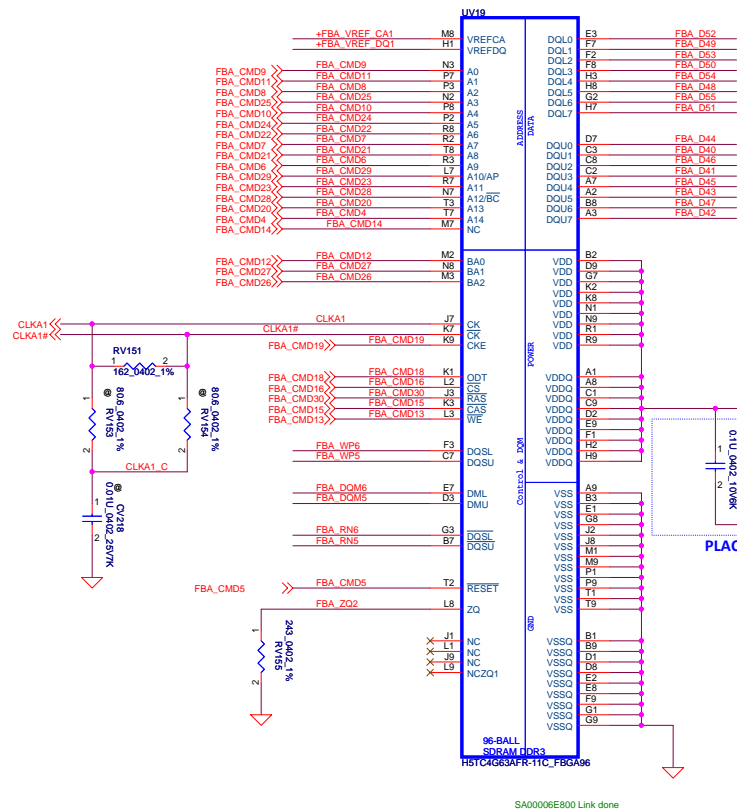


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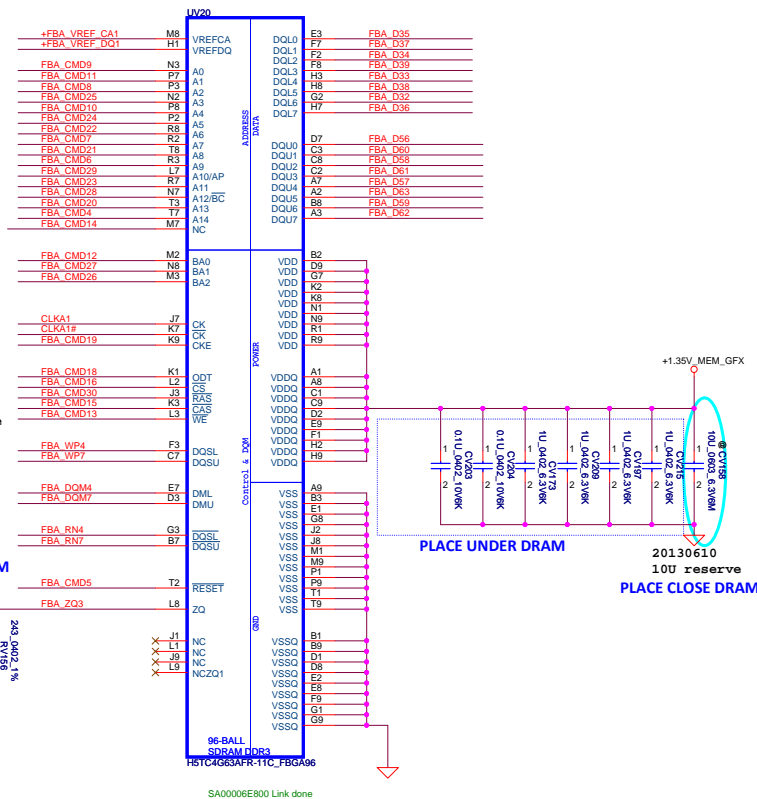
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FBA\_D[32..63] <<>> FBA\_D[32..63]  
 FBA\_WP[4..7] <<>> FBA\_WP[4..7]  
 FBA\_DOM[4..7] <<>> FBA\_DOM[4..7]  
 FBA\_RN[4..7] <<>> FBA\_RN[4..7]

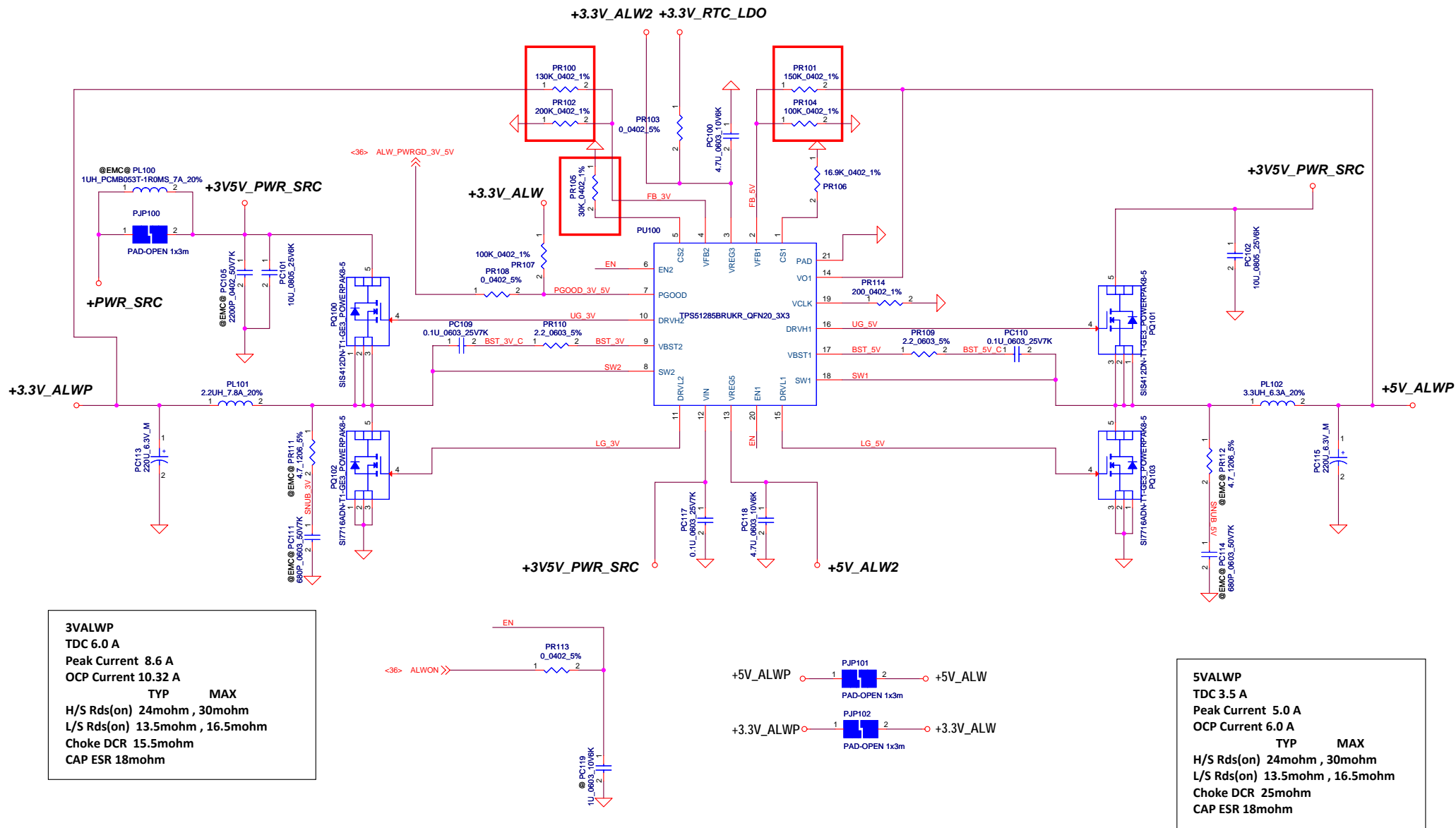


20130610  
10U reserve  
PLACE UNDER DRAM  
PLACE CLOSE DRAM









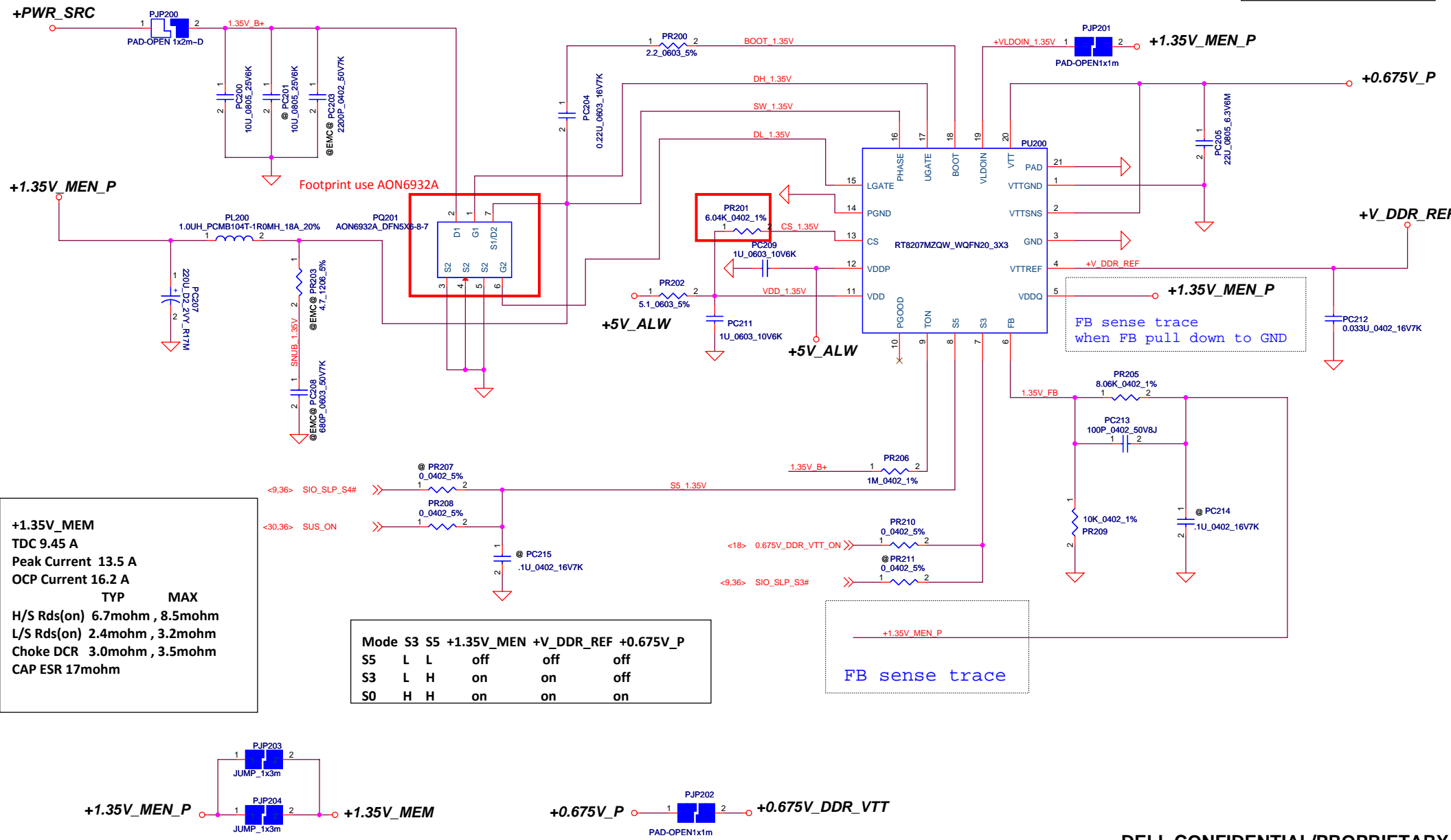
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0.675Volt +/- 5%  
TDC 0.7 A  
Peak Current 1.0 A  
OCP Current 1.2 A




**+1.35V\_MEM**  
TDC 9.45 A  
Peak Current 13.5 A  
OCP Current 16.2 A

	TYP	MAX
H/S Rds(on)	6.7mohm	8.5mohm
L/S Rds(on)	2.4mohm	3.2mohm
Choke DCR	3.0mohm	3.5mohm
CAP ESR	17mohm	

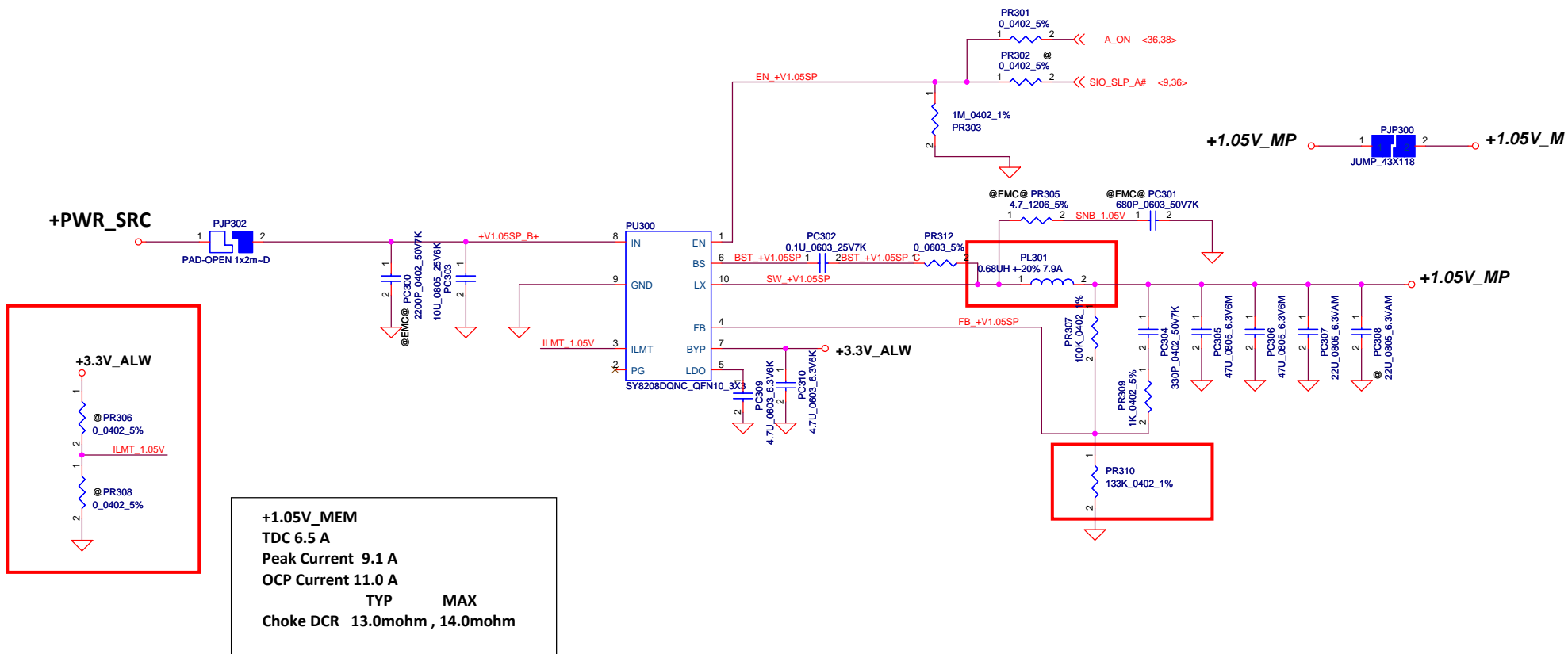
Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

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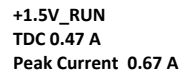
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Vboot=Vvref\*(Rref2/(Rref1+Rboot))  
 Rt=Rrefadj // (Rboot+Rref2)  
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$   
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} / R_{refadj}) + R_{boot} + R_{ref2}]$   
 $V_{out} = V_{min} + N * V_{step}$   
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

#### PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage level	96	96	20
Rrefadj	PR9	39K	20K
Rref1	PR5	39K	20K
Rboot	PR8	1.5K	2K
PR10	30K	18K	24K
Rref2=PR10+PR12	PR12	1.5K	0
C	PC8	1.5nf	2.7nf

Module model information:  
 RT8813A\_V1A for IC module  
 RT8813A\_V1B for SW module

Current Limit threshold setting  
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10uA$   
 $I_{ripple} = (19-0.9) * 0.9 / (304.89KHz * 0.36 * 19) = 7.811A$   
 $OCP = 54A/2 = 27A$  per phase  
 $I_{valley} = 27A - 7.811A/2 = 23.1A$

H-side MOS:TPCA8065  
 Rds(on):  
 11.7mohm @ Vgs=10V  
 9.4mohm @ Vgs=4.5V  
 Id :16A @ Ta=25 degC

L-side MOS:TPCA8057  
 Rds(on):  
 2.0mohm @ Vgs=10V  
 2.6-3.2mohm @ Vgs=4.5V  
 Id :42A @ Ta=25 degC

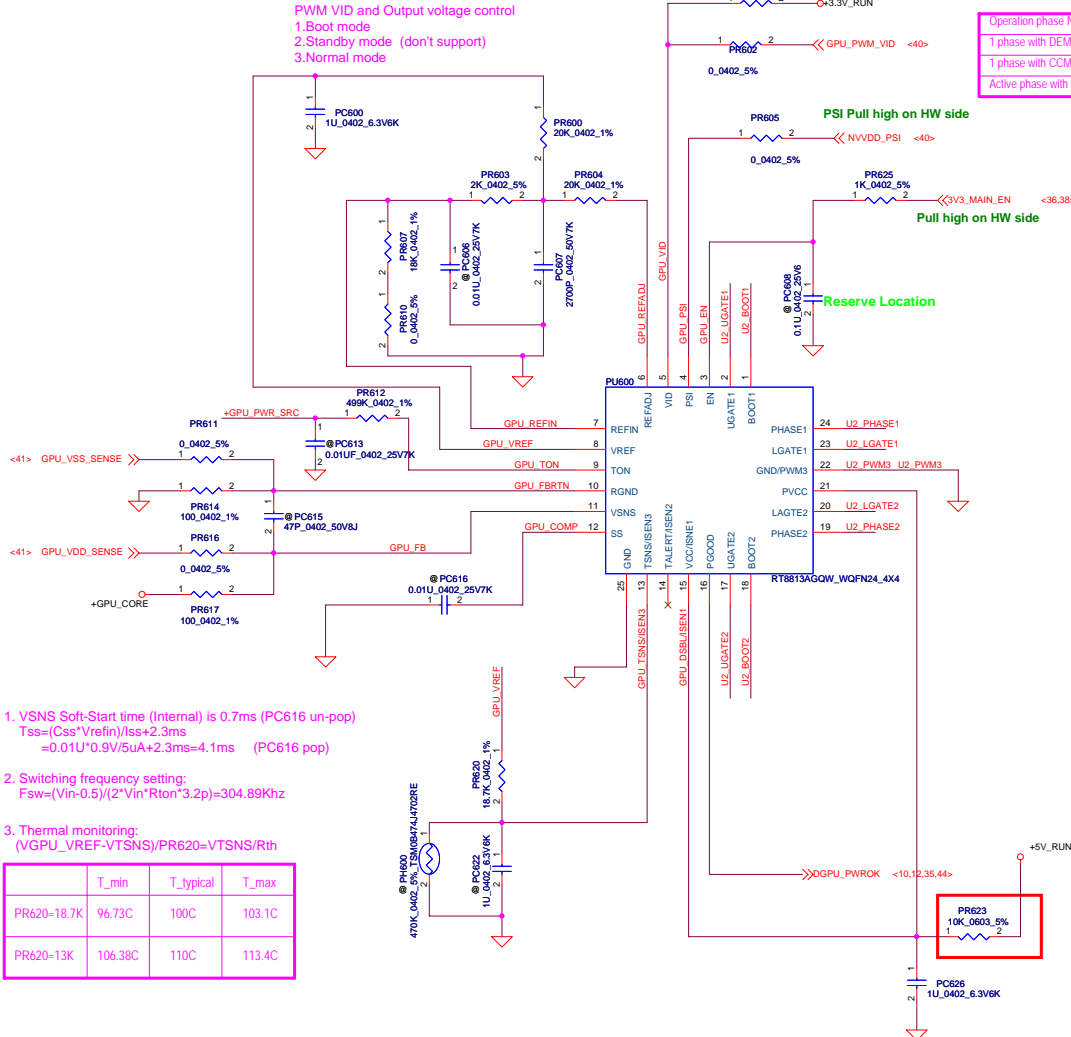
Choke: 0.36uH (Size:10\*10\*4)  
 Rdc=1.1mohm +-5%  
 Heat Rating Current=30A  
 Saturation Current=50A

C=3\*330uF (9mohm)=990uF  
 $V_{ripple} = ripple * ESR(min) = 7.811A * 3mohm = 23.4mV$

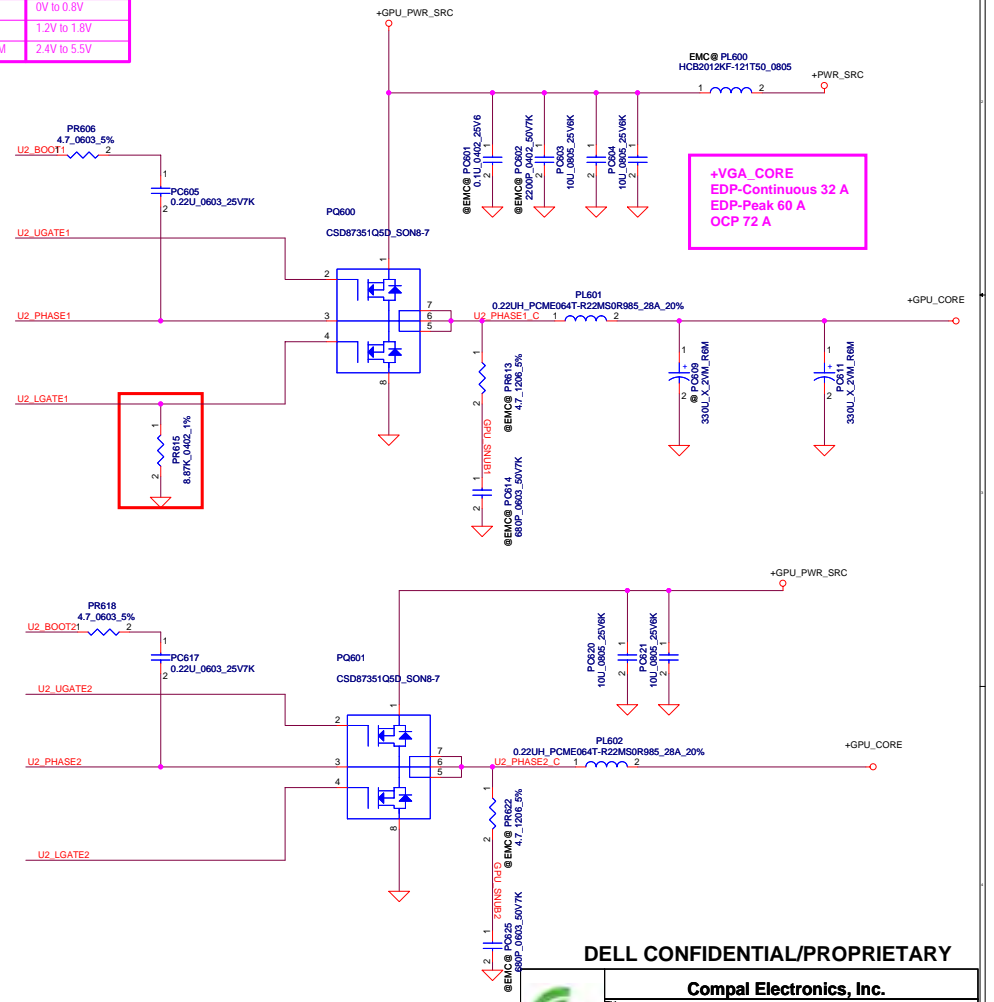
#### Different VGA Chip (different EDP-Mux) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL

PWM VID and Output voltage control  
 1.Boot mode  
 2.Standby mode (don't support)  
 3.Normal mode



Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V



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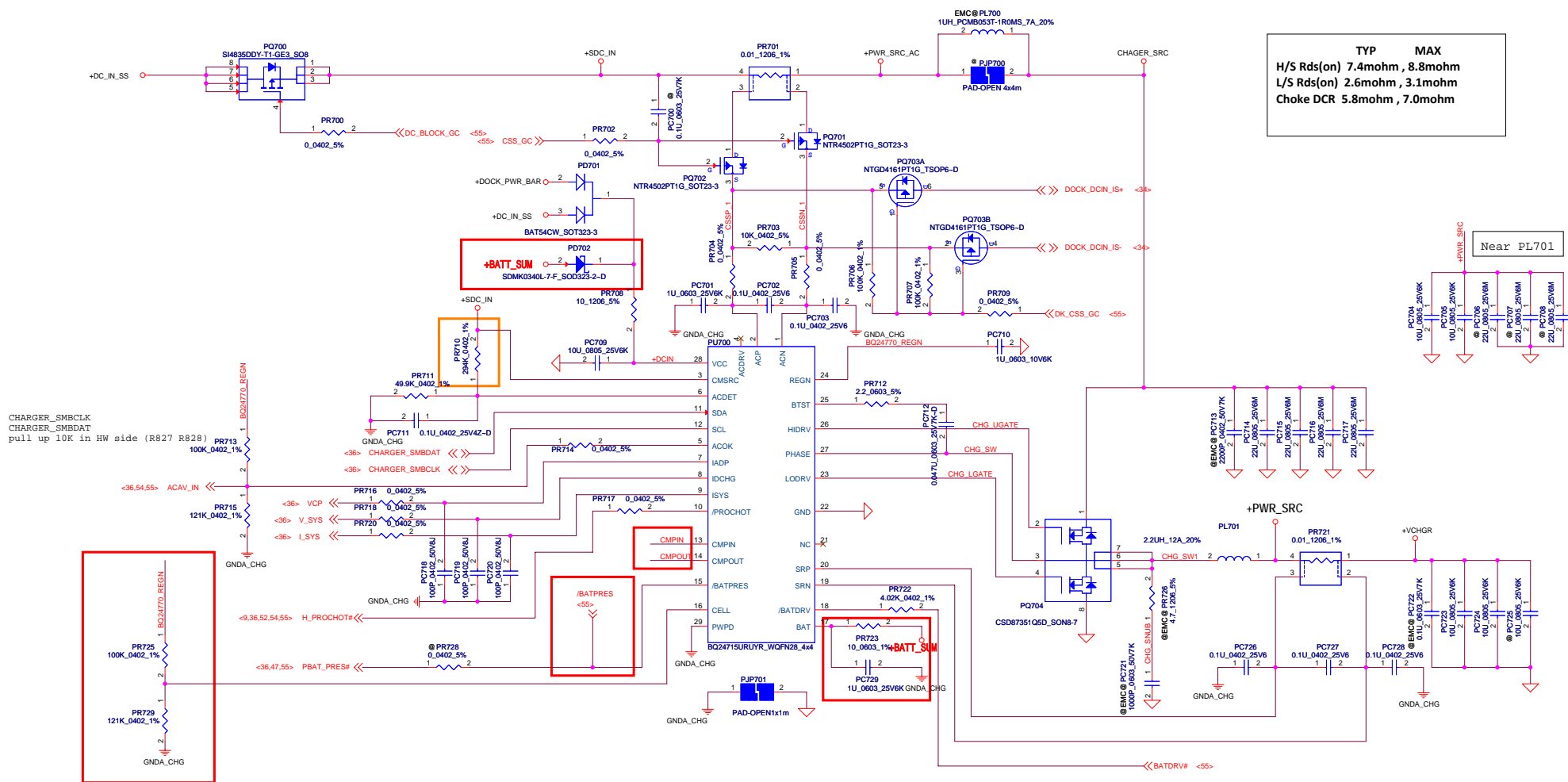
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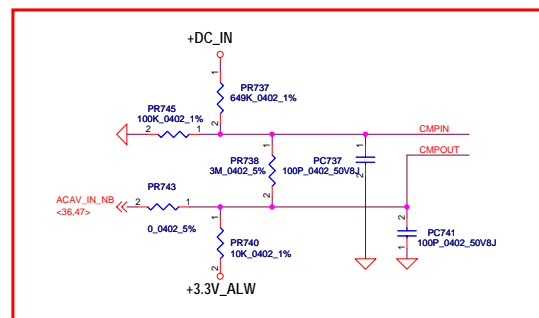
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TYP	MAX
H/S Rds(on)	7.4mohm , 8.8mohm
L/S Rds(on)	2.6mohm , 3.1mohm
Choke DCR	5.8mohm , 7.0mohm



Near PL701

CHARGER\_SMBCLK  
CHARGER\_SMBDAT  
pull up 10K in HW side (R827 R828)



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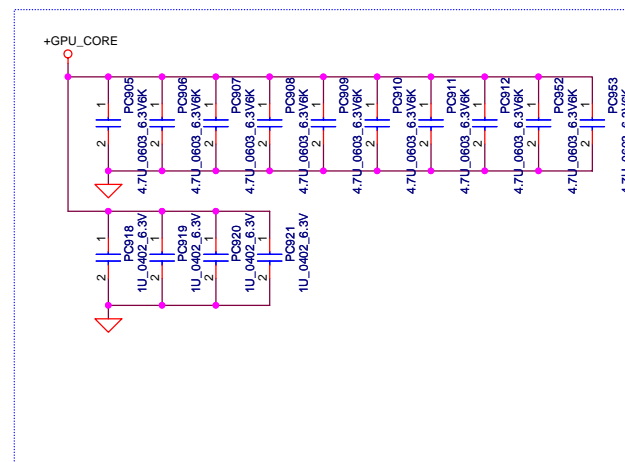
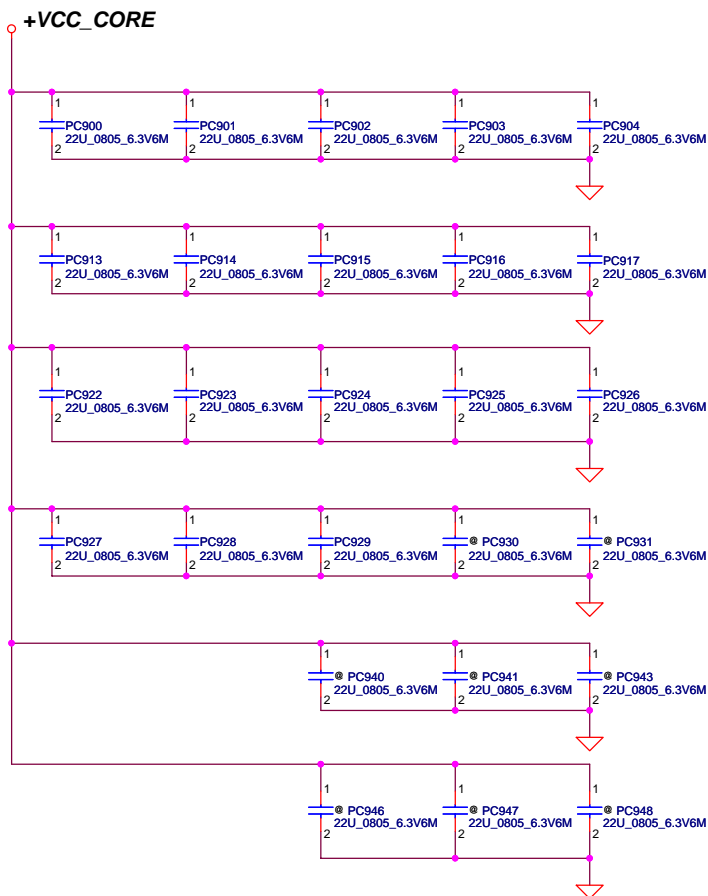
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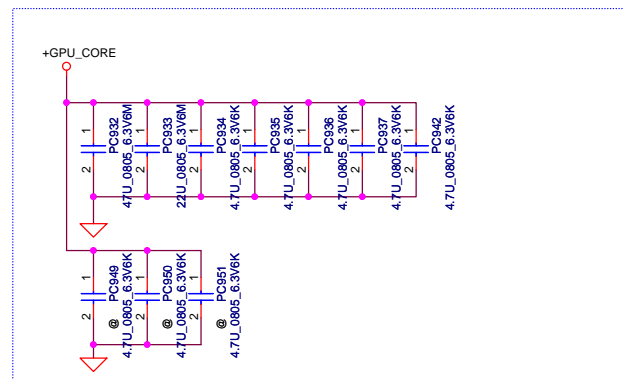
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nVidia GB4-64 package  
Under GPU  
4.7uF 0603 \* 10  
1uF 0402 \* 4



nVidia GB4-64 package  
Near GPU  
47uF 0805 \*1  
22uF 0805 \*1  
4.7uF 0805 \*5

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